1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J92 MLB NEWARK - DVT

11/21/2014

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ALIASES RESOLVED

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PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00107	1	SCHEM,MLB-NEWARK,J92	SCH	CRITICAL	
820-00045	1	PCBF,MLB-NEWARK,J92	PCB	CRITICAL	

DRAWING TITLE: <PART_DESCRIPTION>

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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,CCSAK,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS,EQ:4CH
MLB_MISC	CAM_FREQ:24M,CAM_XTAL:NO,EDP,RSMRST:SMC,PGOOD8:SLP_S4,SSD_LPSR:S3
MLB_DEBUG:ENG	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PVT	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PROD	XDP

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DRAM:HYN_2GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_2GB
DRAM:HYN_4GB_QDP	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB_QDP
DRAM:HYN_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_4GB
DRAM:HYN_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:HYNIX_8GB
DRAM:ELP_2GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_2GB
DRAM:ELP_4GB_QDP	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB_QDP
DRAM:ELP_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_4GB
DRAM:ELP_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4638	1	IC,MCU,LPC11U37,128KB/12KB,TFBGA48	U4600	CRITICAL	HPM:BLANK
341S00190	1	IC,HPM (VXXX) DVT,X261	U4600	CRITICAL	HPM:PROG
338S1231	1	IC,SMC12-B1,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00031	1	IC,SMC-B1,EXTERNAL (VXXXX) PROTO2A, J92	U5000	CRITICAL	SMC:PROG
335S1009	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_WIN:BLANK
335S1010	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S1029	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MIC:BLANK
341S00191	1	EFI ROM,MLB (VXXX) DVT,X261	U6100	CRITICAL	BOOTROM:PROG
335S0948	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLBGA	U8800	CRITICAL	SSDROM_WIN:BLANK
335S0966	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLCSP	U8800	CRITICAL	SSDROM_MAC:BLANK
341S00091	1	S1-X SSD BOOTROM, UI64	U8800	CRITICAL	SSDROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00054	1	IC,CPU,BW,Q0SKZ,Q8,E0,2/2,0.8,4.5W,.8,B1234	U0500	CRITICAL	CPU:0.8GHZ
337S00099	1	IC,CPU,BW,QH2Z,PRQ,F0,2/2,1.1,5W,.85,B1234	U0500	CRITICAL	CPU:1.1GHZ
337S00098	1	IC,CPU,BW,QH2V,PRQ,F0,2/2,1.2,5W,.9,B1234	U0500	CRITICAL	CPU:1.2GHZ
337S00097	1	IC,CPU,BW,QH2R,PRQ,F0,2/2,1.3,5W,.9,B1234	U0500	CRITICAL	CPU:1.3GHZ
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7995	1	LABEL,BARCODE,2D,1D,CONFIG,MLB,X261	LABEL		

SSD POP Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S0243	1	POP,S1-X CONTROLLER+4GBITS ELP,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_ELP
339S0244	1	POP,S1-X CONTROLLER+4GBITS HYN,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_HYN
685-00003	1	POP,MLB,S1X-A1,ELP-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_ELP
685-00004	1	POP,MLB,S1X-A1,HYN-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_HYN
338S1288	1	IC,S1-X,CONTROLLER,A1,841(312)B,FCCSP	SSD_CTRL	CRITICAL	S1X:A1
338S00055	1	IC,S1-X,CONTROLLER,A2,841(312)B,FCBGA	SSD_CTRL	CRITICAL	S1X:A2
333S0733	1	IC,LPDDR2,128MX32,1.2V,ELPIDA 28NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:ELPIDA
333S0694	1	IC,LPDDR2,128MX32,1.2V,HYNIX 29NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:HYNIX
870-00878	1	TAPE,CONDUCTIVE,SSD,REEL,X261	SSD_TAPE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-6486	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S00028	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB_QDP
998-6453	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_2GB
998-6454	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB_QDP
333S0730	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0731	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0740	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0741	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_8GB

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CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
2GB	0	0
4GB QDP	0	1
4GB DDP	1	0
8GB	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00074	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
128S0393	128S0334		ALL	Kemet alt to Sanyo
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
197S0590	197S0588		ALL	Epson alt to TXC
197S0591	197S0588		ALL	NDK alt to TXC
107S0249	107S0251		ALL	TFT alt to Cyntec
138S0789	138S0941		ALL	Samsung alt to Murata
333S0700	333S0704		ALL	Hynix CAM DRAM alt to Elpida
333S00016	333S0704		ALL	Elpida new die CAM DRAM alt
333S00030	333S0704		ALL	Hynix new die CAM DRAM alt
339S0243	339S0244		ALL	Elpida SSD DRAM alt to Hynix
335S0948	335S0966		ALL	Winbond alt to Macronix
128S0631	128S0351		ALL	NEC alt to Sanyo
128S00008	128S0380		ALL	NEC alt to Sanyo
311S00007	311S0426		ALL	Sanyo alt to NEC
311S00008	311S0271		ALL	Samsung alt to Murata
311S00018	311S0409		ALL	Diodes alt to NXP
740S00004	740S0134		ALL	Kemet alt to Sanyo
740S00005	740S0190		ALL	Polytronics alt to Wayon
128S0296	128S0487		ALL	Sanyo alt to NEC
128S00012	128S0487		ALL	ROHM alt to NEC
128S00025	128S0469		ALL	Kemet alt to Sanyo
128S0374	128S0469		ALL	NEC alt to Sanyo
376S00007	376S1179		ALL	AOS alt to Vishay
376S1080	376S0820		ALL	Diodes alt to OnSemi
376S00036	376S1194		ALL	Vishay alt to OnSemi
376S00037	376S1193		ALL	Vishay alt to OnSemi
685-00004	685-00003	SSDRAM:A1_ELP	ALL	Hynix SSD DRAM alt to Elpida
337S00061	337S00054	CPU:0.8GHZ	ALL	2.4G turbo CPU alt to 2.0G

SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

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BOM Configuration

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Top level BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-6568	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6569	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6570	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6571	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6572	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6573	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6574	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6575	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6576	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6577	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6578	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6579	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6580	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6581	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6582	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6583	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6584	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6585	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6586	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6587	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6588	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6589	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6590	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6591	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6592	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6593	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6594	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6595	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6596	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6597	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6598	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6599	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6600	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6601	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6602	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6603	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6604	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6605	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6606	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6607	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6608	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6609	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6610	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6611	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6612	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6613	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6614	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6615	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP

Partial & development BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00014	CMN PTS,PCBA,MLB-NEWARK,J92	MLB_COMMON
685-00003	POP,MLB,S1X-A2,ELP-4GBIT,X261	S1X:A2,S1X_DRAM:ELPIDA
685-00004	POP,MLB,S1X-A2,HYN-4GBIT,X261	S1X:A2,S1X_DRAM:HYNIX
939-00043	PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261	ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP

Common BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00014	1	CMN PTS,PCBA,MLB-NEWARK,J92	CMNPTS	CRITICAL	CMN

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00196	1	BT ROM (VXX) DVT,2MBIT,X261	U3570	CRITICAL	BT:PROG
341S00197	1	WIFI ROM (PXXXX) DVT,WW1,X261	U3580	CRITICAL	WIFI:FCC
341S00198	1	WIFI ROM (PXXXX) DVT,WW2,X261	U3580	CRITICAL	WIFI:ETSI
341S00199	1	WIFI ROM (PXXXX) DVT,WW3,X261	U3580	CRITICAL	WIFI:APAC
341S00200	1	WIFI ROM (PXXXX) DVT,IND,X261	U3580	CRITICAL	WIFI:IND

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG

SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE
J92 BOM Variants

Apple Inc.

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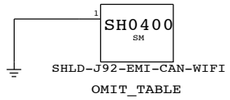
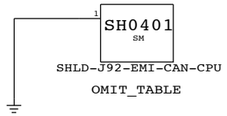
WIFI EMI CAN



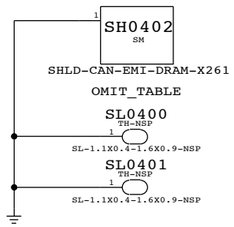
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-7064	1	CAN,EMI,WIFI,X261	SH0400	CRITICAL	

CPU EMI CAN



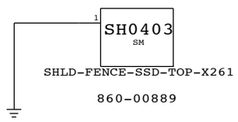
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00112	1	CAN,EMI,CPU,X261	SH0401	CRITICAL	

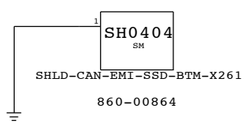
DRAM EMI CAN & SLOTs



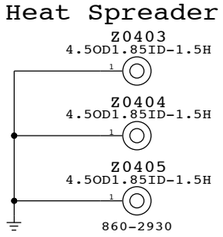
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00400	1	CAN,EMI,DRAM,TALL,X261	SH0402	CRITICAL	

SSD EMI FENCE & CAN

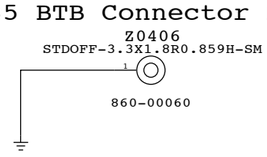




CPU Heat Spreader Bosses



E85 BTB Connector Boss



SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE
PD PARTS

Apple Inc.

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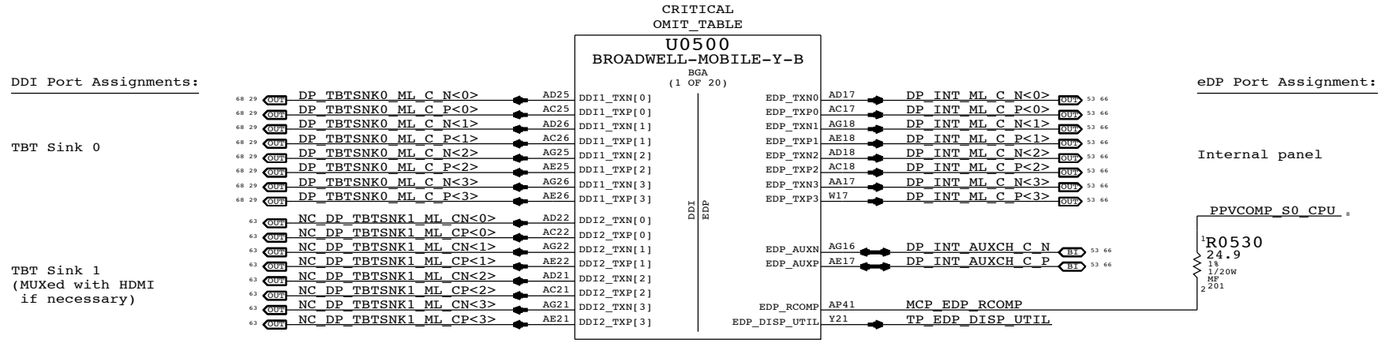

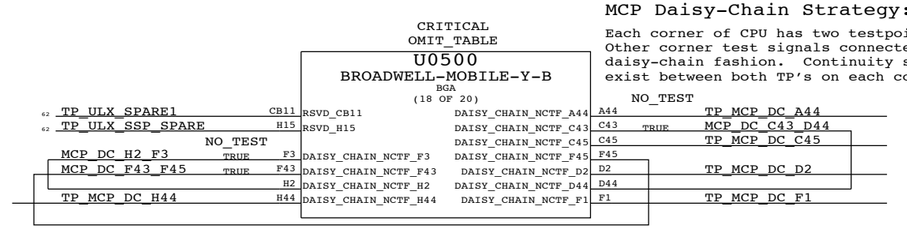

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

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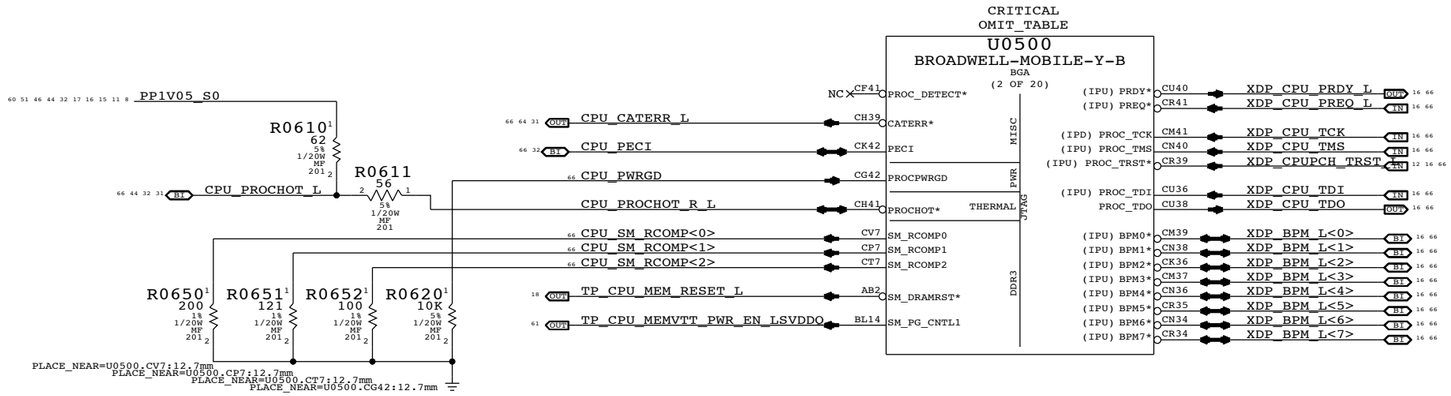
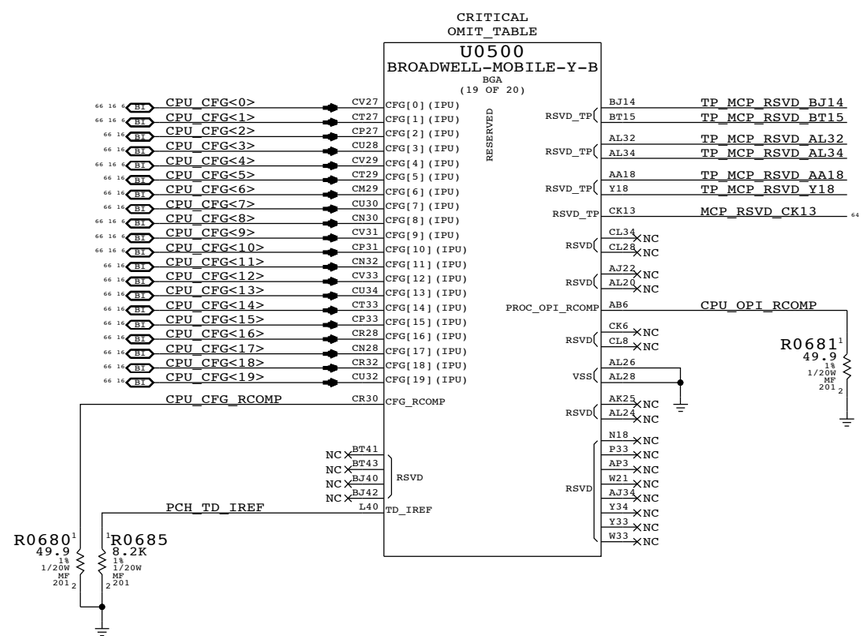
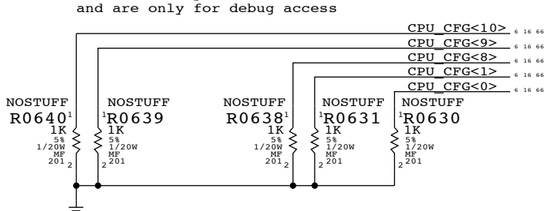


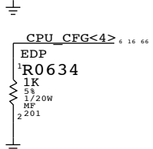


TBD: Confirm w/ Intel which still apply for BDW-Y

CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access





SYNC_MASTER=J92 WILL SYNC_DATE=04/10/2013

PAGE TITLE
CPU Misc/JTAG/CFG/RSVD

Apple Inc.

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CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(3 OF 20)

MEMORY CHANNEL A

MEM_A_DQ<0>	CT17	SA_DQ0	
MEM_A_DQ<1>	CV17	SA_DQ1	
MEM_A_DQ<2>	CN14	SA_DQ2	
MEM_A_DQ<3>	CP15	SA_DQ3	
MEM_A_DQ<4>	CN16	SA_DQ4	
MEM_A_DQ<5>	CR16	SA_DQ5	
MEM_A_DQ<6>	CM13	SA_DQ6	
MEM_A_DQ<7>	CV15	SA_DQ7	
MEM_A_DQ<8>	CT13	SA_DQ8	
MEM_A_DQ<9>	CP13	SA_DQ9	
MEM_A_DQ<10>	CP10	SA_DQ10	
MEM_A_DQ<11>	CM10	SA_DQ11	
MEM_A_DQ<12>	CN12	SA_DQ12	
MEM_A_DQ<13>	CV13	SA_DQ13	
MEM_A_DQ<14>	CV10	SA_DQ14	
MEM_A_DQ<15>	CT10	SA_DQ15	
MEM_A_DQ<16>	CT25	SA_DQ16	
MEM_A_DQ<17>	CP25	SA_DQ17	
MEM_A_DQ<18>	CN22	SA_DQ18	
MEM_A_DQ<19>	CP23	SA_DQ19	
MEM_A_DQ<20>	CN24	SA_DQ20	
MEM_A_DQ<21>	CV25	SA_DQ21	
MEM_A_DQ<22>	CV23	SA_DQ22	
MEM_A_DQ<23>	CT23	SA_DQ23	
MEM_A_DQ<24>	CN20	SA_DQ24	
MEM_A_DQ<25>	CN18	SA_DQ25	
MEM_A_DQ<26>	CT21	SA_DQ26	
MEM_A_DQ<27>	CT19	SA_DQ27	
MEM_A_DQ<28>	CP19	SA_DQ28	
MEM_A_DQ<29>	CP21	SA_DQ29	
MEM_A_DQ<30>	CV19	SA_DQ30	
MEM_A_DQ<31>	CV21	SA_DQ31	
MEM_A_DQ<32>	BU2	SA_DQ32	
MEM_A_DQ<33>	BW2	SA_DQ33	
MEM_A_DQ<34>	BW6	SA_DQ34	
MEM_A_DQ<35>	BU4	SA_DQ35	
MEM_A_DQ<36>	BW4	SA_DQ36	
MEM_A_DQ<37>	BT3	SA_DQ37	
MEM_A_DQ<38>	BU6	SA_DQ38	
MEM_A_DQ<39>	BT5	SA_DQ39	
MEM_A_DQ<40>	BN2	SA_DQ40	
MEM_A_DQ<41>	BR2	SA_DQ41	
MEM_A_DQ<42>	BN6	SA_DQ42	
MEM_A_DQ<43>	BN4	SA_DQ43	
MEM_A_DQ<44>	BR6	SA_DQ44	
MEM_A_DQ<45>	BR4	SA_DQ45	
MEM_A_DQ<46>	BM5	SA_DQ46	
MEM_A_DQ<47>	BM3	SA_DQ47	
MEM_A_DQ<48>	BT11	SA_DQ48	
MEM_A_DQ<49>	BU10	SA_DQ49	
MEM_A_DQ<50>	BW12	SA_DQ50	
MEM_A_DQ<51>	BW10	SA_DQ51	
MEM_A_DQ<52>	BW8	SA_DQ52	
MEM_A_DQ<53>	BU8	SA_DQ53	
MEM_A_DQ<54>	BU12	SA_DQ54	
MEM_A_DQ<55>	BT9	SA_DQ55	
MEM_A_DQ<56>	BN8	SA_DQ56	
MEM_A_DQ<57>	BR8	SA_DQ57	
MEM_A_DQ<58>	BN12	SA_DQ58	
MEM_A_DQ<59>	BN10	SA_DQ59	
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MEM_A_DQ<61>	BR10	SA_DQ61	
MEM_A_DQ<62>	BM11	SA_DQ62	
MEM_A_DQ<63>	BM9	SA_DQ63	

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SA_CLK0	CG2	MEM_A_CLK_P<0>	
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SA_CLK1	CC6	MEM_A_CLK_P<1>	
SA_CKE0	CH11	MEM_A_CKE<0>	
SA_CKE1	CH9	MEM_A_CKE<1>	
SA_CKE2	CA12	MEM_A_CKE<2>	
SA_CKE3	CA10	MEM_A_CKE<3>	
SA_CS0*	CA4	MEM_A_CS_L<0>	
SA_CS1*	CA2	MEM_A_CS_L<1>	
SA_ODT0	CA6	MEM_A_ODT<0>	
SA_CAB3	CE2	=MEM_A_RAS_L	
SA_CAB2	CE4	=MEM_A_WE_L	
SA_CAB1	CC8	=MEM_A_CAS_L	
SA_CAB4	CB5	=MEM_A_BA<0>	
SA_CAB6	CC2	MEM_A_CAB<6>	
SA_CAA5	CF11	=MEM_A_BA<2>	
SA_CAB9	CE8	=MEM_A_A<0>	
SA_CAB8	CE12	=MEM_A_A<1>	
SA_CAB5	CF5	=MEM_A_A<2>	
	CE10	TP_LPDDR3_RSVD1	
NOTUSED	CG8	TP_LPDDR3_RSVD2	
SA_CAA0	CG6	=MEM_A_A<5>	
SA_CAA2	CH3	=MEM_A_A<6>	
SA_CAA4	CE6	=MEM_A_A<7>	
SA_CAA3	CB9	=MEM_A_A<8>	
SA_CAA1	CC12	=MEM_A_A<9>	
SA_CAB7	CF3	=MEM_A_A<10>	
SA_CAA7	CG12	=MEM_A_A<11>	
SA_CAA6	CH5	MEM_A_CAA<6>	
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SA_DQSN1	CR12	MEM_A_DQS_N<1>	
SA_DQSN2	CR24	MEM_A_DQS_N<2>	
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SA_DQSP2	CU24	MEM_A_DQS_P<2>	
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SM_VREF_CA	AP13	CPU_DIMM_VREFCA	
SM_VREF_DQ0	AU14	CPU_DIMMA_VREFDQ	
SM_VREF_DQ1	AT13	CPU_DIMMB_VREFDQ	
SM_VCCDDQG	CC14	TP_ULX_DDR_VCCDDQG	

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(4 OF 20)

MEMORY CHANNEL B

MEM_B_DQ<0>	BK3	SB_DQ0	
MEM_B_DQ<1>	BK5	SB_DQ1	
MEM_B_DQ<2>	BG6	SB_DQ2	
MEM_B_DQ<3>	BJ2	SB_DQ3	
MEM_B_DQ<4>	BJ4	SB_DQ4	
MEM_B_DQ<5>	BJ6	SB_DQ5	
MEM_B_DQ<6>	BG2	SB_DQ6	
MEM_B_DQ<7>	BG4	SB_DQ7	
MEM_B_DQ<8>	BF3	SB_DQ8	
MEM_B_DQ<9>	BF5	SB_DQ9	
MEM_B_DQ<10>	BC6	SB_DQ10	
MEM_B_DQ<11>	BE2	SB_DQ11	
MEM_B_DQ<12>	BE4	SB_DQ12	
MEM_B_DQ<13>	BE6	SB_DQ13	
MEM_B_DQ<14>	BC2	SB_DQ14	
MEM_B_DQ<15>	BC4	SB_DQ15	
MEM_B_DQ<16>	BE10	SB_DQ16	
MEM_B_DQ<17>	BC10	SB_DQ17	
MEM_B_DQ<18>	BE8	SB_DQ18	
MEM_B_DQ<19>	BC8	SB_DQ19	
MEM_B_DQ<20>	BF11	SB_DQ20	
MEM_B_DQ<21>	BC12	SB_DQ21	
MEM_B_DQ<22>	BE12	SB_DQ22	
MEM_B_DQ<23>	BF9	SB_DQ23	
MEM_B_DQ<24>	BJ12	SB_DQ24	
MEM_B_DQ<25>	BG12	SB_DQ25	
MEM_B_DQ<26>	BJ8	SB_DQ26	
MEM_B_DQ<27>	BJ10	SB_DQ27	
MEM_B_DQ<28>	BG8	SB_DQ28	
MEM_B_DQ<29>	BG10	SB_DQ29	
MEM_B_DQ<30>	BK9	SB_DQ30	
MEM_B_DQ<31>	BK11	SB_DQ31	
MEM_B_DQ<32>	AM1	SB_DQ32	
MEM_B_DQ<33>	AH2	SB_DQ33	
MEM_B_DQ<34>	AJ3	SB_DQ34	
MEM_B_DQ<35>	AM5	SB_DQ35	
MEM_B_DQ<36>	AM3	SB_DQ36	
MEM_B_DQ<37>	AJ1	SB_DQ37	
MEM_B_DQ<38>	AJ5	SB_DQ38	
MEM_B_DQ<39>	AH4	SB_DQ39	
MEM_B_DQ<40>	AG3	SB_DQ40	
MEM_B_DQ<41>	AG1	SB_DQ41	
MEM_B_DQ<42>	AD2	SB_DQ42	
MEM_B_DQ<43>	AE3	SB_DQ43	
MEM_B_DQ<44>	AE1	SB_DQ44	
MEM_B_DQ<45>	AG5	SB_DQ45	
MEM_B_DQ<46>	AD4	SB_DQ46	
MEM_B_DQ<47>	AE5	SB_DQ47	
MEM_B_DQ<48>	AM9	SB_DQ48	
MEM_B_DQ<49>	AM7	SB_DQ49	
MEM_B_DQ<50>	AH8	SB_DQ50	
MEM_B_DQ<51>	AJ9	SB_DQ51	
MEM_B_DQ<52>	AM11	SB_DQ52	
MEM_B_DQ<53>	AJ7	SB_DQ53	
MEM_B_DQ<54>	AJ11	SB_DQ54	
MEM_B_DQ<55>	AH10	SB_DQ55	
MEM_B_DQ<56>	AE11	SB_DQ56	
MEM_B_DQ<57>	AG7	SB_DQ57	
MEM_B_DQ<58>	AE7	SB_DQ58	
MEM_B_DQ<59>	AE9	SB_DQ59	
MEM_B_DQ<60>	AG11	SB_DQ60	
MEM_B_DQ<61>	AG9	SB_DQ61	
MEM_B_DQ<62>	AD8	SB_DQ62	
MEM_B_DQ<63>	AD10	SB_DQ63	

SB_CK0*	AW6	MEM_B_CLK_N<0>	
SB_CK0	AW4	MEM_B_CLK_P<0>	
SB_CK1*	AP11	MEM_B_CLK_N<1>	
SB_CK1	AP9	MEM_B_CLK_P<1>	
SB_CKE0	BA2	MEM_B_CKE<0>	
SB_CKE1	BA4	MEM_B_CKE<1>	
SB_CKE2	AR8	MEM_B_CKE<2>	
SB_CKE3	AP5	MEM_B_CKE<3>	
SB_CS0*	AR10	MEM_B_CS_L<0>	
SB_CS1*	AT11	MEM_B_CS_L<1>	
SB_ODT0	AU10	MEM_B_ODT<0>	
SB_CAB3	BA10	=MEM_B_RAS_L	
SB_CAB2	AW12	=MEM_B_WE_L	
SB_CAB1	AW10	=MEM_B_CAS_L	
SB_CAB4	AY11	=MEM_B_BA<0>	
SB_CAB6	BA12	MEM_B_CAB<6>	
SB_CAA5	AU2	=MEM_B_BA<2>	
SB_CAB9	AT9	=MEM_B_A<0>	
SB_CAB8	AR4	=MEM_B_A<1>	
SB_CAB5	AU8	=MEM_B_A<2>	
	AR6	TP_LPDDR3_RSVD3	
NOTUSED	AT5	TP_LPDDR3_RSVD4	
SB_CAA0	AT3	=MEM_B_A<5>	
SB_CAA2	BA8	=MEM_B_A<6>	
SB_CAA4	AY3	=MEM_B_A<7>	
SB_CAA3	AW2	=MEM_B_A<8>	
SB_CAA1	AY5	=MEM_B_A<9>	
SB_CAB7	AY9	=MEM_B_A<10>	
SB_CAA7	AU4	=MEM_B_A<11>	
SB_CAA6	AU6	MEM_B_CAA<6>	
SB_CAB0	AW8	=MEM_B_A<13>	
SB_CAA9	BA6	=MEM_B_A<14>	
SB_CAA8	AR2	=MEM_B_A<15>	
SB_DQSN0	BH5	MEM_B_DQS_N<0>	
SB_DQSN1	BD5	MEM_B_DQS_N<1>	
SB_DQSN2	BD11	MEM_B_DQS_N<2>	
SB_DQSN3	BH11	MEM_B_DQS_N<3>	
SB_DQSN4	AK2	MEM_B_DQS_N<4>	
SB_DQSN5	AF2	MEM_B_DQS_N<5>	
SB_DQSN6	AK8	MEM_B_DQS_N<6>	
SB_DQSN7	AF8	MEM_B_DQS_N<7>	
SB_DQSP0	BH3	MEM_B_DQS_P<0>	
SB_DQSP1	BD3	MEM_B_DQS_P<1>	
SB_DQSP2	BD9	MEM_B_DQS_P<2>	
SB_DQSP3	BH9	MEM_B_DQS_P<3>	
SB_DQSP4	AK4	MEM_B_DQS_P<4>	
SB_DQSP5	AF4	MEM_B_DQS_P<5>	
SB_DQSP6	AK10	MEM_B_DQS_P<6>	
SB_DQSP7	AF10	MEM_B_DQS_P<7>	

SYNC MASTER=J92 LS MLB SYNC DATE=07/17/2013

PAGE TITLE
CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(12 OF 20)
BRW ULX POWER

1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)

69 60 59 52 46 21 20 19 10 PP1V2_S3 — CT3
TP_MCP_DC_CY3 — CY3
CB1, BV1, CF1, BA14, CL1, CM3
TP_MCP_DC_CW1 — CW1
AP1, AV1, BB1, BC14, BE14, BF1, BK1, BP1, CR1 — VDDQ
NC CJ32, NC CM33 — RSVD

60 45 35 10 8 PPVCC_S0_CPU
R0860[1] 100 5% 1/20W MF 201
PLACE_NEAR=U0500.CH45:50.8mm
45 35 10 8 PPVCC_S0_CPU — AV45 VCC
NC CJ28 RSVD
66 44 OUT CPU_VCCSENSE_P — CH45 VCC_SENSE
TP_PPVCCIO_S0_CPU — NC AL16 RSVD
Max load: 300mA — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V — BM43 VCCIO_OUT
5 PPVCOMP_S0_CPU — Max load: 300mA — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V — AR40 VCOMP_OUT
NC AL22, NC AK33, NC CL14 — RSVD

51 46 44 32 17 16 15 11 8 6 60 PP1V05_S0
R0800[1] 75 1% 1/20W MF 201
R0802[1] 130 1% 1/20W MF 201
R0810 43 5% 1/20W MF 201
R0811 0 5% 1/20W MF 0201
R0812 0 5% 1/20W MF 0201
66 44 IN CPU_VIDALERT_L — CPU_VIDALERT_R_L — CD43 VIDALERT*
66 44 OUT CPU_VIDSCLK — CPU_VIDSCLK_R — CD41 VIDSCLK
CPU_VIDSOUT_R — CE40 VIDSOUT
66 44 BI CPU_VIDSOUT
CPU_VCCST_PWRGD — 46 17 16 IN — BU14 VCCST_PWRGD
44 OUT CPU_VR_EN — CE42 VR_EN
CPU_VR_READY — CF43 VR_READY
R0802.2: PLACE_NEAR=U0500.CE40:2.54mm
R0810.2: PLACE_NEAR=U0500.CD43:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
R0850[1] 10K 5% 1/20W MF 201
16 IN CPU_PWR_DEBUG_L — CK40 PWR_DEBUG*
CF39, CK40, CJ20 — VSS
62 44 IN
TP_MCP_RSVD_CJ22 — CJ22
TP_MCP_RSVD_CK23 — CK23 — RSVD_TP
TP_IVR_ERROR — CK27 IVR_ERROR
TP_IST_TRIGGER — CL26 IST_TRIGGER
NC CK21, NC CL22, NC CK25, NC CM27, NC CK19, NC CJ16, NC CK31 — RSVD
51 46 44 32 17 16 15 11 8 6 60 PP1V05_S0 — ???mA Max — AJ20 VCCST

PPVCC_S0_CPU 8 10 35 45 60 — 32A Max
BK45, CB41, CA40, BY41, BW40, CY17, AY45, BB45, BD45, BF45, BH45, BT45, BV45, BY45, CB45, CD45, CF45, CM45, CN44, CR43, CR45, CU44, CV43, CV45, CY19, CY21, CY23, CY25, CY27, CY29, CY31, CY33, CY36, CY38, CY42, CY44, BM45, BP45, CA44, BV41, BV43, BW44, CY40, CY13, CY15, BW42, BY43, CA42, CB43 — VCC
CV45 — MCP_DC_CV45 64
CY44 — TP_MCP_DC_CY44

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
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60 51 11 PP1V05_S0SW_PCH_PCIE — AB38, W45, AA45 — VCCPCIEPHY
60 51 11 PP1V05_S0SW_PCH_SATA — N45, T45 — VCCSATAPHY
60 51 11 PP1V05_S0SW_PCH_USB3 — AC45, AD36, AE45 — VCCUSB3PHY
17 16 15 11 8 6 60 51 46 44 32 PP1V05_S0 — T31 VCC1_05_PHY
12 11 PP1V05_S0SW_PCH_VCCSATA3PLL — T33 VCCSATA3PLL
14 11 PP1V05_S0SW_PCH_VCCUSB3PLL — T35 VCCUSB3PLL
11 8 PP1V05_S0_PCH_VCCAPLL_OPI — AK19, AK29 — VCCOPIPLL, VCCHDAPLL
60 51 48 46 16 12 11 8 PP1V05_SUS — U30 DCPSUS3
60 46 40 17 11 8 PP1V5_S0 — W1, AA13 — VCCHDA
60 51 48 46 16 12 11 8 PP1V05_SUS — AG14 DCPSUS2
29 28 27 18 15 14 11 8 60 51 46 PP3V3_SUS — U18 VCCSUS3_3
33 22 17 16 15 13 11 8 75 73 60 59 51 47 46 37 PP3V3_S5 — AA1, AB14 — VCCDSW3_3
23 18 75 72 69 53 47 46 40 36 35 34 33 32 29 24 PP3V3_S0 — A30, A28, A26, T27 — VCC3_3
11 PP1V05_S0_PCH_VCC_ICC — AL37 VCCCLK4
12 11 PP1V05_S0_PCH_VCCACLKPLL — AK35 VCCACLKPLL
17 16 15 11 8 6 60 51 46 44 32 PP1V05_S0 — AL30 VCCCLK6
AK31 VCCCLK2
AJ26 VCCCLK7
AL39 VCCCLK5
AJ28 VCCCLK3
AK23 VCCCLK1
29 28 27 18 15 14 11 8 60 51 46 PP3V3_SUS — AL14 VCCSUS3_3

RTC: VCCSUS3_3_RTC AC15 PP3V3_SUS; VCCRTC AA15; DCPRTC V15 PPVOUT_S0_PCH_DCPRTC (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V)
SPI: VCCSPI A24 PP3V3_SUS, T25
HSIO: VCCASW AE15 PP1V05_S0; Y22 PP1V05_S0
OPI
USB3
CORE: VCC1_05 W22, AJ16, AH36, AG45, AJ45, T17
AZALIA/HDA
VRM/USB2/AZALIA: DCPSUSBYP AG13 PP1V05_S5_PCH_VCCDSW (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V); VCCASW N1, T1, W14 PP1V05_S0
MISC: DCPSUS1 U16 PP1V05_SUS
THERMAL SENSOR: VCCTS1_5 AJ32 PP1V5_S0; VCCTS3_3 AB36 PP3V3_S0
GPIO/LCC: SERIAL IO: VCCSDIO A32 PP3V3_S0
SUS OSCILLATOR: DCPSUS4 T21 PP1V05_SUS_PCH_VCCAOSCSUS 11
ICC: VCCUSB2PLL AK17 PP1V05_S0_PCH_VCCAPLL_OPI 8 11
USB2: VCC1_05_USB AE13 PP1V05_S0 6 8 11 15 16 17 32 44 46 51 60
WPT LP POWER

PPVRTC_G3H 12 13 46 60
C0892 0.1UF 10% 10V X5R-CERM 0201
C0891 0.1UF 10% 10V X5R-CERM 0201
C0890 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AA15::6.35mm
C0895 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U0500.AA15::6.35mm
BYPASS=U0500.V15::6.35mm
PP3V3_S5 8 11 13 15 16 17 22 33 37 46 47 51 59 60 73 75
C0897 0.47UF 10% 6.3V CERM-X5R 0201
PLACE_NEAR=U0500.AG13:6.35mm
R0896 0 5% 1/20W MF 0201
PP1V05_S5_PCH_VCCDSW_R (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.1 mm, VOLTAGE=1.05V)
C0896 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AG13::6.35mm

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PAGE TITLE: CPU/PCH POWER
Apple Inc.
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BRANCH: <BRANCH>
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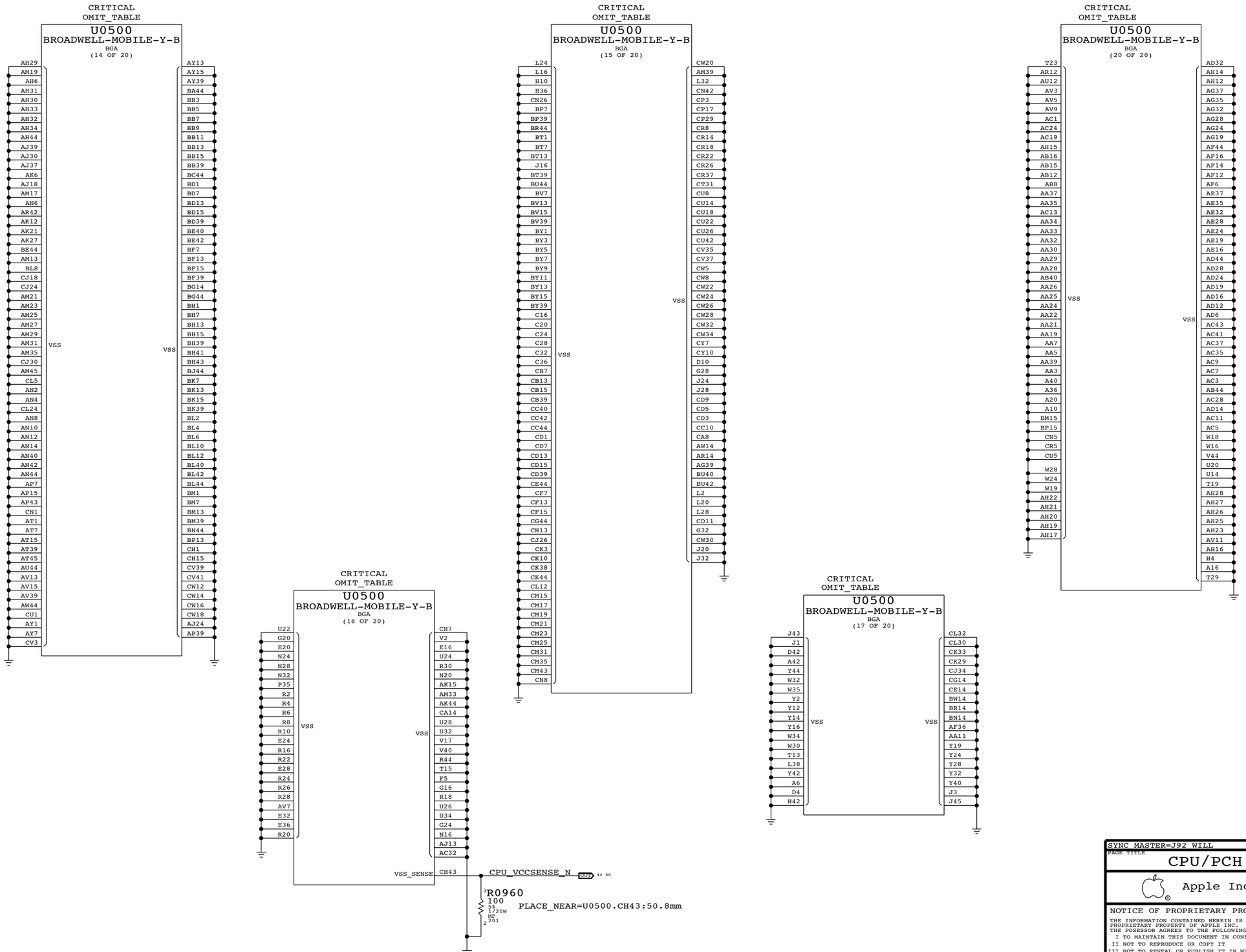

SYNC MASTER=J92 WILL SYNC DATE=04/10/2013

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CPU/PCH GROUNDS

Apple Inc.

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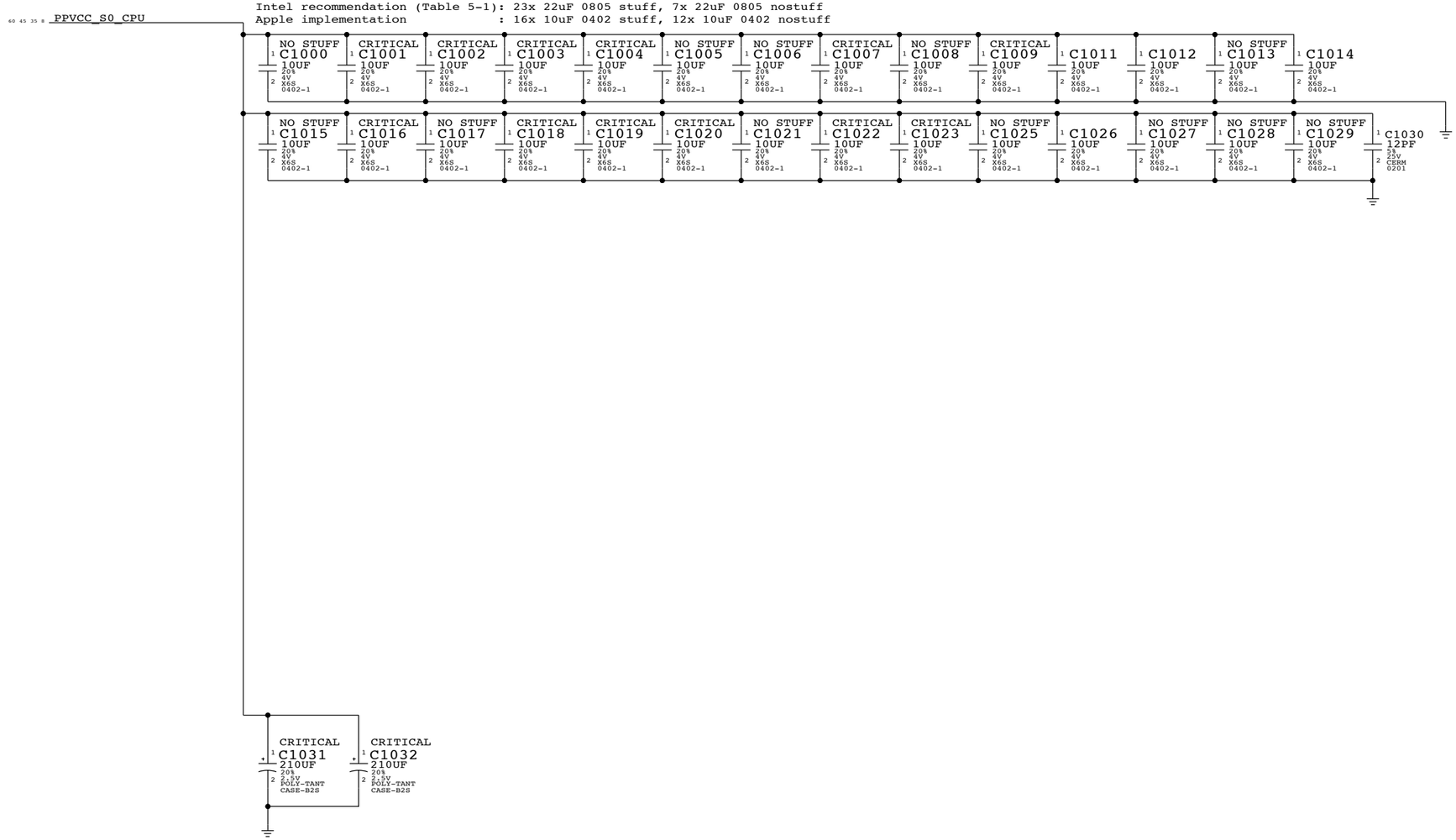
All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

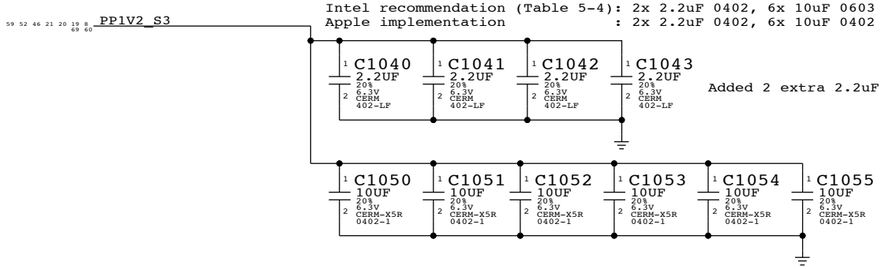
CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 16x 10uF 0402 stuff, 12x 10uF 0402 nostuff



CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402



Added 2 extra 2.2uF per Harris Beach v0.9 schematic

SYNC MASTER=J92 DEVMLB SYNC DATE=10/01/2013

PAGE TITLE
CPU Decoupling

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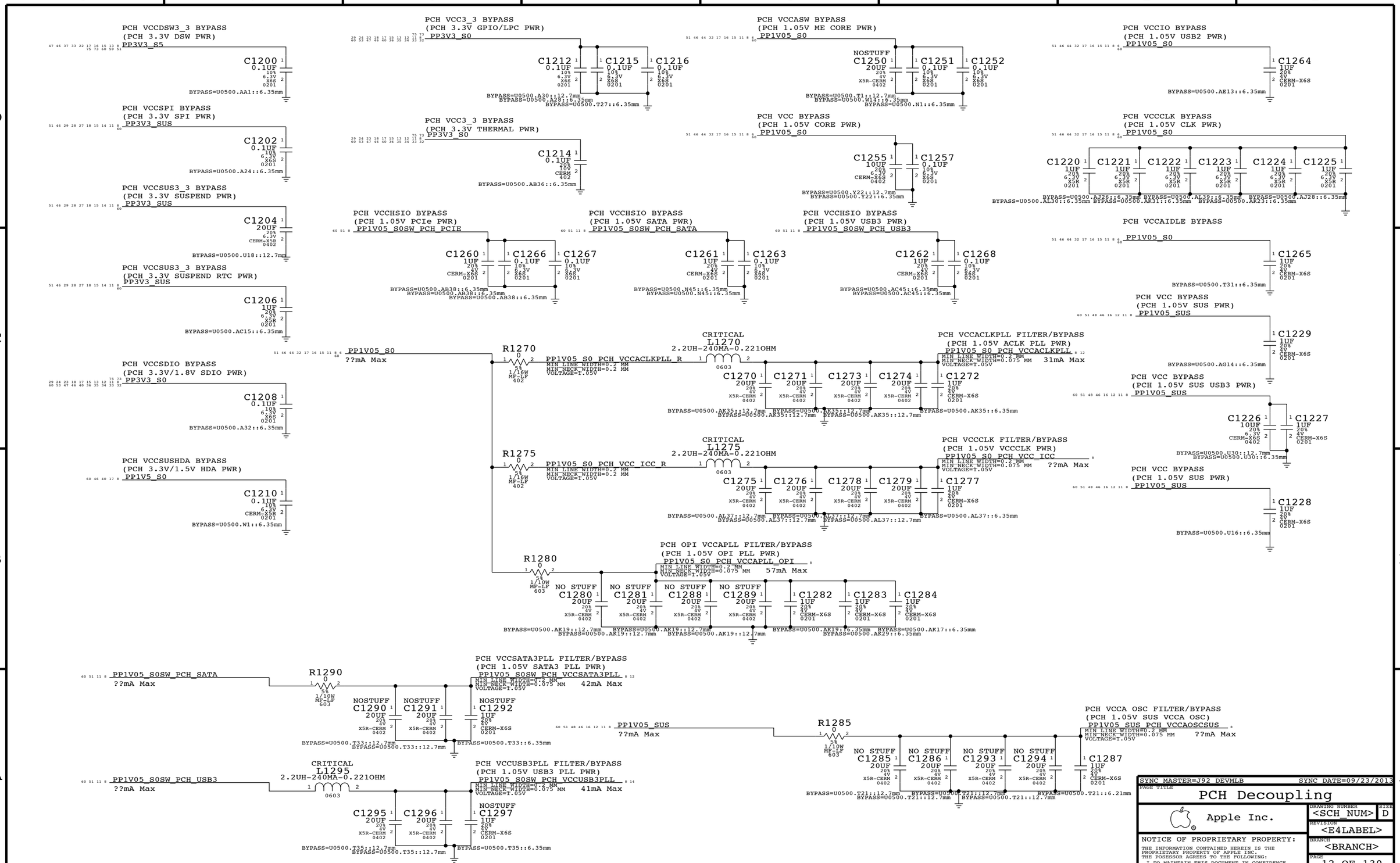
PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
C1200 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AA1::6.35mm
PCH VCC3_3 BYPASS
(PCH 3.3V GIO/LPC PWR)
PP3V3_S0
C1212 0.1UF 10% 6.3V X6S 0201
C1215 0.1UF 10% 6.3V X6S 0201
C1216 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A30::12.7mm
BYPASS=U0500.A28::6.35mm
BYPASS=U0500.T27::6.35mm
PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NOSTUFF
C1250 20UF 20% 4V X5R-CERM 0402
C1251 0.1UF 10% 6.3V X6S 0201
C1252 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.T1::12.7mm
BYPASS=U0500.W14::6.35mm
BYPASS=U0500.N1::6.35mm
PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AE13::6.35mm
PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
C1202 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A24::6.35mm
PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 10% 10V CERM 402
BYPASS=U0500.AB36::6.35mm
PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V CERM-X6S 0402
C1257 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.Y22::12.7mm
BYPASS=U0500.Y22::6.35mm
PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1220 1UF 20% 6.3V X5R 0201
C1221 1UF 20% 6.3V X5R 0201
C1222 1UF 20% 6.3V X5R 0201
C1223 1UF 20% 6.3V X5R 0201
C1224 1UF 20% 6.3V X5R 0201
C1225 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AJ26::6.35mm
BYPASS=U0500.AL39::6.35mm
BYPASS=U0500.AJ28::6.35mm
BYPASS=U0500.AL30::6.35mm
BYPASS=U0500.AK31::6.35mm
BYPASS=U0500.AK23::6.35mm
PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.U18::12.7mm
PCH VCCHSIO BYPASS
(PCH 1.05V PCIe PWR)
PP1V05_S0SW_PCH_PCIE
C1260 1UF 20% 4V CERM-X6S 0201
C1266 0.1UF 10% 6.3V X6S 0201
C1267 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AB38::6.35mm
BYPASS=U0500.AB39::6.35mm
BYPASS=U0500.AB38::6.35mm
PCH VCCHSIO BYPASS
(PCH 1.05V SATA PWR)
PP1V05_S0SW_PCH_SATA
C1261 1UF 20% 4V CERM-X6S 0201
C1263 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.N45::6.35mm
BYPASS=U0500.N45::6.35mm
PCH VCCHSIO BYPASS
(PCH 1.05V USB3 PWR)
PP1V05_S0SW_PCH_USB3
C1262 1UF 20% 4V CERM-X6S 0201
C1268 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AC45::6.35mm
BYPASS=U0500.AC45::6.35mm
PCH VCCAIDLE BYPASS
PP1V05_S0
C1265 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T31::6.35mm
PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AC15::6.35mm
PCH VCC BYPASS
(PCH 1.05V SUS PWR)
PP1V05_SUS
C1229 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AG14::6.35mm
PP1V05_S0
??mA Max
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.2210HM 0603
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max
C1270 20UF 20% 4V X5R-CERM 0402
C1271 20UF 20% 4V X5R-CERM 0402
C1273 20UF 20% 4V X5R-CERM 0402
C1274 20UF 20% 4V X5R-CERM 0402
C1272 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::6.35mm
PCH VCC BYPASS
(PCH 1.05V SUS USB3 PWR)
PP1V05_SUS
C1226 10UF 20% 6.3V CERM-X6S 0402
C1227 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.U30::12.7mm
BYPASS=U0500.U30::6.35mm
PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A32::6.35mm
R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.2210HM 0603
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
C1275 20UF 20% 4V X5R-CERM 0402
C1276 20UF 20% 4V X5R-CERM 0402
C1278 20UF 20% 4V X5R-CERM 0402
C1279 20UF 20% 4V X5R-CERM 0402
C1277 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::6.35mm
PCH VCC BYPASS
(PCH 1.05V SUS PWR)
PP1V05_SUS
C1228 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.U16::6.35mm
PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0
C1210 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U0500.W1::6.35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max
R1280 0 5% 1/10W MF-LF 603
NO STUFF
C1280 20UF 20% 4V X5R-CERM 0402
NO STUFF
C1281 20UF 20% 4V X5R-CERM 0402
NO STUFF
C1288 20UF 20% 4V X5R-CERM 0402
NO STUFF
C1289 20UF 20% 4V X5R-CERM 0402
C1282 1UF 20% 4V CERM-X6S 0201
C1283 1UF 20% 4V CERM-X6S 0201
C1284 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::6.35mm
BYPASS=U0500.AK29::6.35mm
BYPASS=U0500.AK17::6.35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max
PP1V05_S0SW_PCH_SATA
??mA Max
R1290 0 5% 1/10W MF-LF 603
NOSTUFF
C1290 20UF 20% 4V X5R-CERM 0402
NOSTUFF
C1291 20UF 20% 4V X5R-CERM 0402
NOSTUFF
C1292 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T33::12.7mm
BYPASS=U0500.T33::12.7mm
BYPASS=U0500.T33::6.35mm
PP1V05_SUS
??mA Max
R1285 0 5% 1/10W MF-LF 603
PCH VCCA OSC FILTER/BYPASS
(PCH 1.05V SUS VCCA OSC)
PP1V05_SUS_PCH_VCCAOSCSUS
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
NO STUFF
C1285 20UF 20% 4V X5R-CERM 0402
NO STUFF
C1286 20UF 20% 4V X5R-CERM 0402
NO STUFF
C1293 20UF 20% 4V X5R-CERM 0402
NO STUFF
C1294 20UF 20% 4V X5R-CERM 0402
C1287 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::6.21mm
PP1V05_S0SW_PCH_USB3
??mA Max
CRITICAL
L1295 2.2UH-240MA-0.2210HM 0603
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max
C1295 20UF 20% 4V X5R-CERM 0402
C1296 20UF 20% 4V X5R-CERM 0402
NOSTUFF
C1297 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T35::12.7mm
BYPASS=U0500.T35::12.7mm
BYPASS=U0500.T35::6.35mm
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.
SYNC MASTER=J92 DEVMLB
SYNC DATE=09/23/2013
PAGE TITLE
PCH Decoupling
Apple Inc.
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<SCH_NUM>
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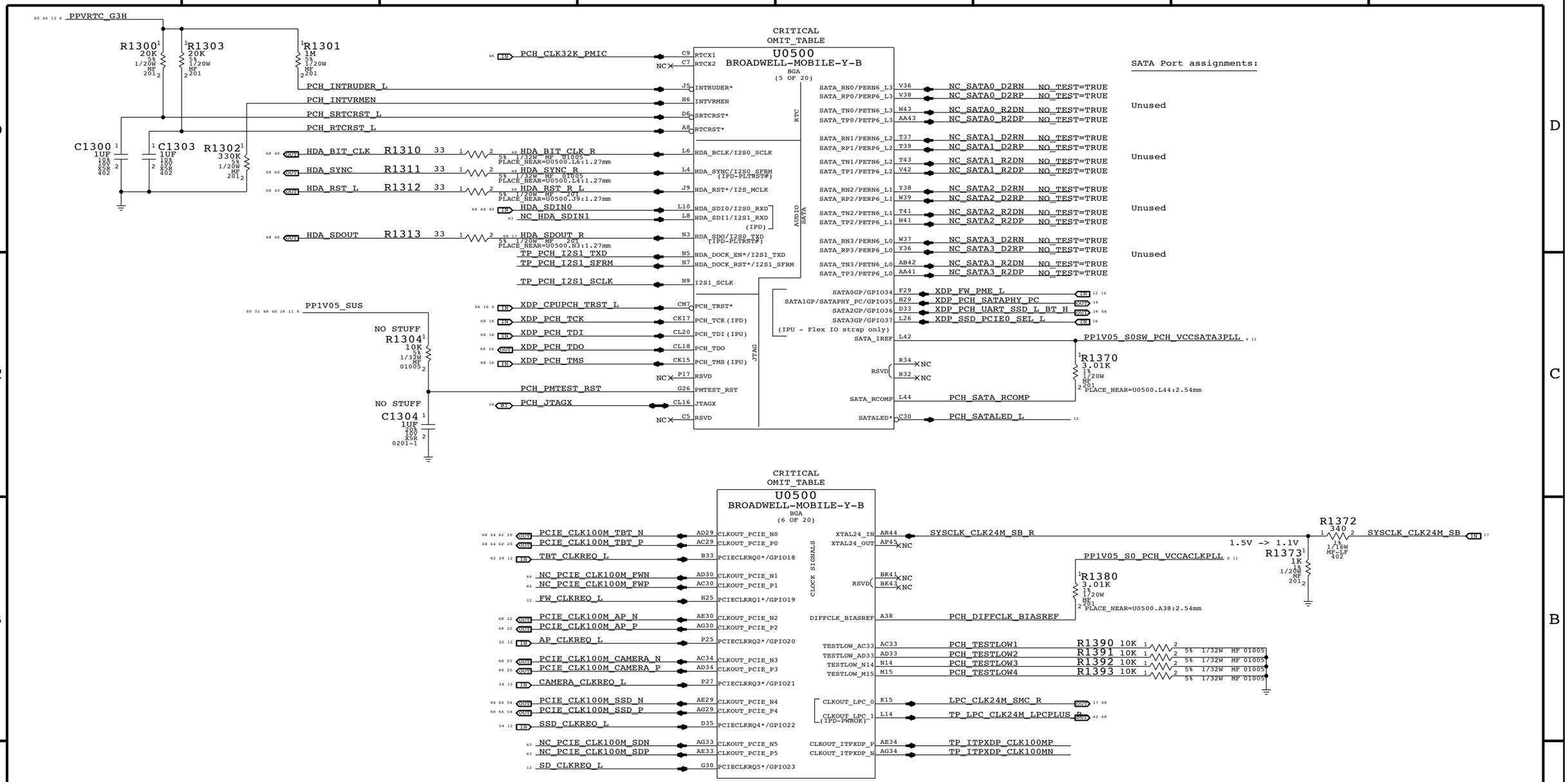

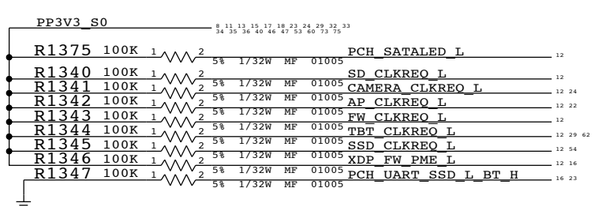

SYNC_MASTER=J92 WILL SYNC_DATE=04/10/2013

PAGE TITLE
PCH Audio/JTAG/SATA/CLK

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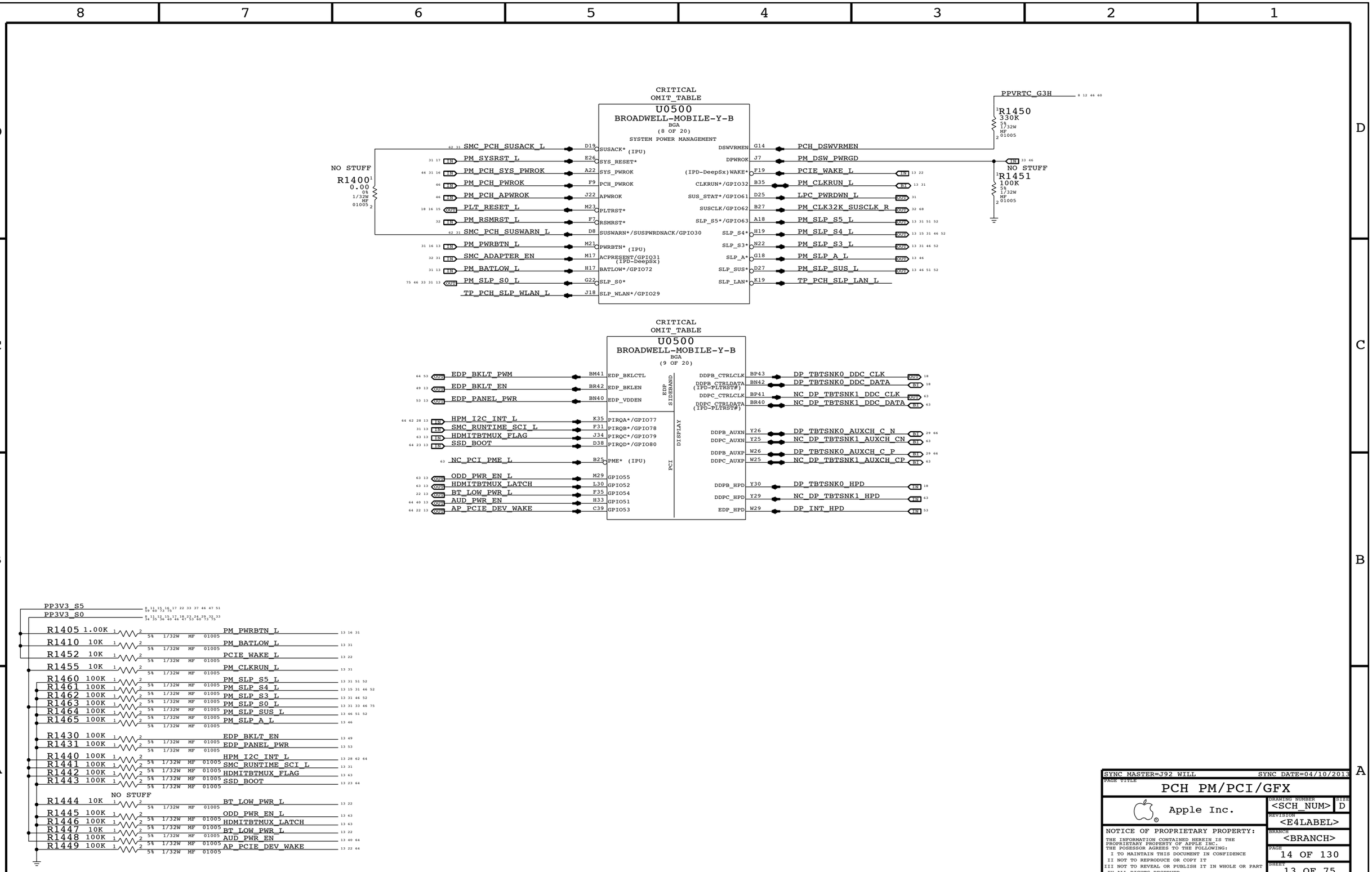

SYNC MASTER=J92 WILL SYNC DATE=04/10/2013

PAGE TITLE

PCH PM/PCI/GFX

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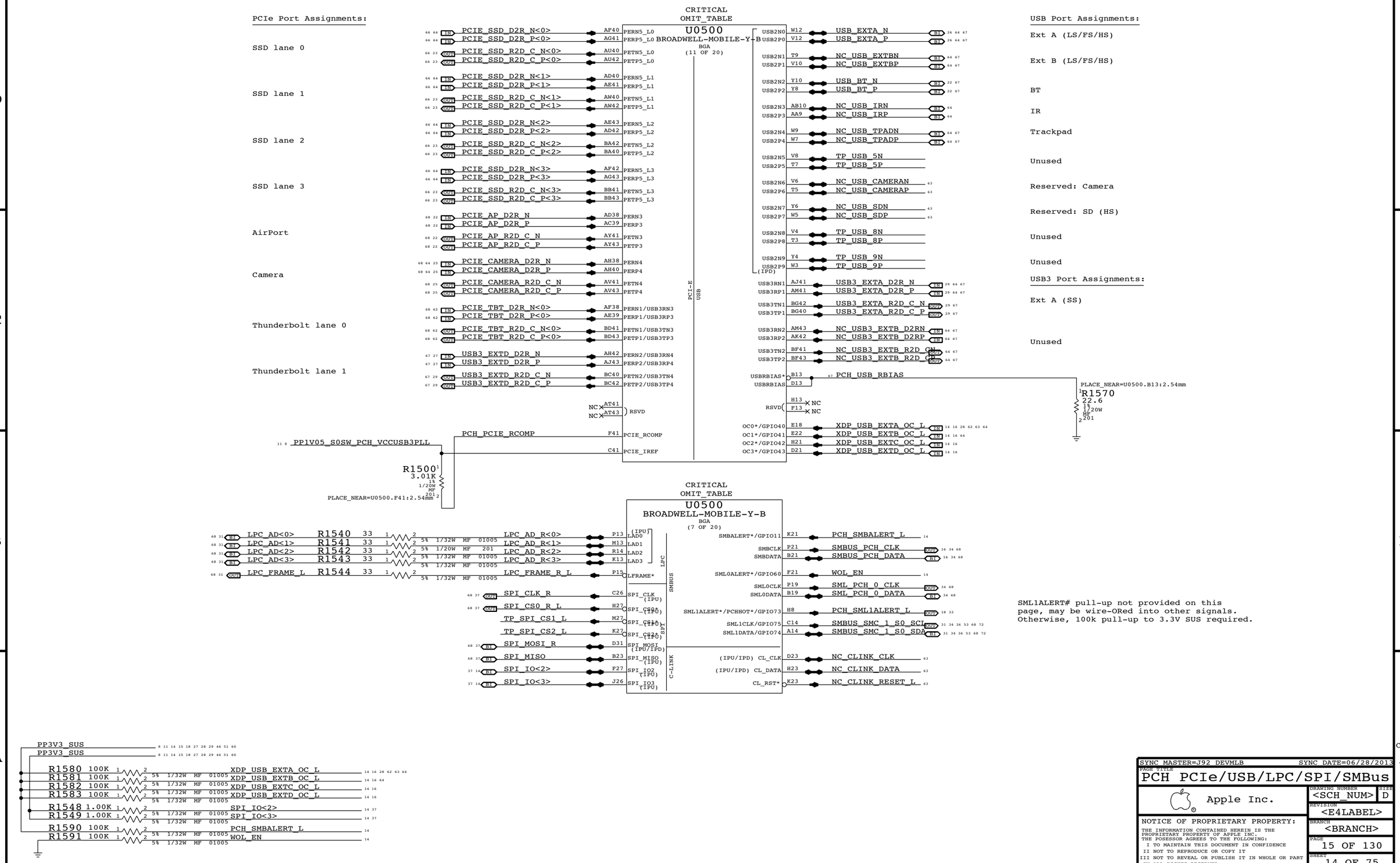

SYNC MASTER=J92 DEVMLB SYNC DATE=06/28/2013

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

SYNC MASTER=J92 DEVMLB SYNC DATE=08/14/2013

PAGE TITLE
PCH GPIO/MISC/LPIO

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Extra BPM Probepoints

XDP_BPM_L<2> — PP1802
XDP_BPM_L<3> — PP1803
XDP_BPM_L<4> — PP1804
XDP_BPM_L<5> — PP1805
XDP_BPM_L<6> — PP1806
XDP_BPM_L<7> — PP1807

Merged (CPU/PCH) Micro2-XDP

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

PP1V05_S0

R1830 150 5% 1/20W MF 201

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG_L	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_TDO — R1810 51 — PP1V05_S0
XDP_CPU_TCK — R1813 51
PLACE_NEAR=U0500.CU38:28mm
PLACE_NEAR=U0500.CM41:28mm
TDI and TMS are terminated in CPU.

CPU_VCCST_PWRGD — R1800 1K — PLACE_NEAR=U0500.BU14:2.54mm
PM_PWRBTN_L — R1802 0 — PLACE_NEAR=U5000.K1:2.54mm
PM_PCH_SYS_PWROK — R1804 0
XDP_CPU_TCK
PCH_JTAGX — R1835 0 — PLACE_NEAR=J1800.58:28mm

R1805 1K — PLT_RESET_L — PLACE_NEAR=U0500.AG7:2.54mm

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/20W MF 201
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

XDP_CPU_PRESENT_L
NOSTUFF
R1832 0 5% 1/20W MF 0201

CRITICAL
Q1840 DMN5L06VK-7 SOT563 — XDP_CPU_TDO — PLACE_NEAR=J1800.55:28mm
Q1840 — XDP_CPUPCH_TRST_L — MAKE_BASE=TRUE
Q1842 — XDP_CPU_TDI
Q1842 — XDP_CPU_TMS

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0		
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	PP1873	
XDP_USB_EXTD_OC_L	PP1874	
XDP_SDCONN_STATE_CHANGE_L	PP1875	
XDP_MLB_RAMCFG1		
XDP_MLB_RAMCFG2		
XDP_MLB_RAMCFG3		
XDP_JTAG_ISP_TCK	PP1879	
XDP_FW_PME_L	PP1880	
XDP_PCH_SATAPHY_PC	R1881 SHORT OMIT NONE NONE NONE 201	PCH_SATAPHY_PC
XDP_PCH_UART_SSD_L_BT_H	R1882 SHORT OMIT NONE NONE NONE 201	PCH_UART_SSD_L_BT_H
XDP_SSD_PCIE0_SEL_L	R1883 1K 5% 1/20W MF 201	
XDP_LPCPLUS_GPIO	PP1884	
XDP_PCH_GPIO17	PP1885	
XDP_PCH_USB3PHY_PC	R1886 SHORT OMIT NONE NONE NONE 201	PCH_USB3PHY_PC
XDP_JTAG_ISP_TDI	PP1887	

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIEx_SEL_L straps are connected via 1K to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 — VCC, A, Y, NC, GND
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST	R1897 51	NO STUFF

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PAGE TITLE: CPU/PCH Merged XDP

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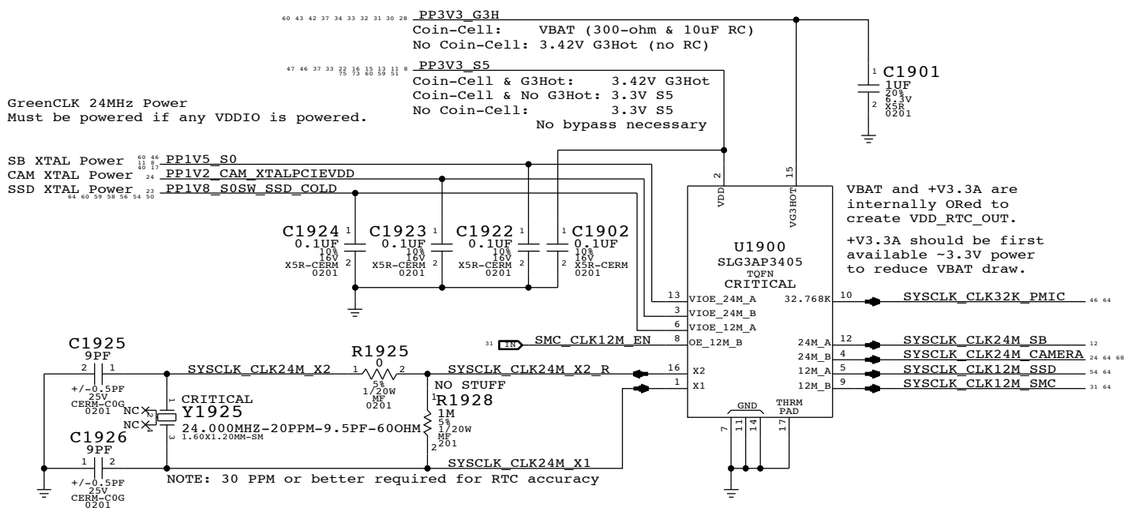
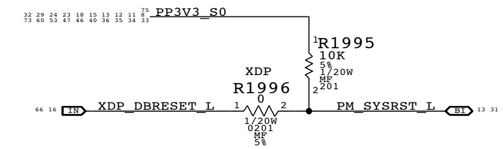
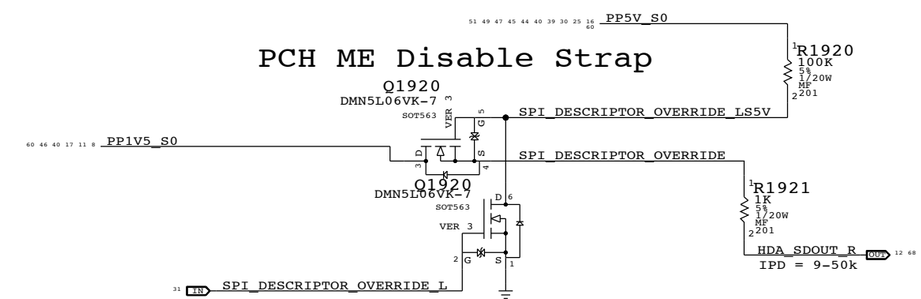
System 32kHz / 12MHz / 24MHz Clock Generator

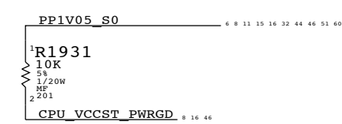




PCH ME Disable Strap

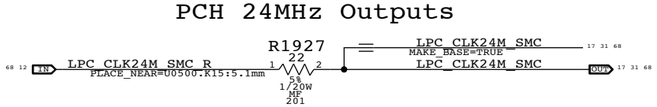


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



www.qdzbwx.com

PCH 24MHz Outputs



SYNC MASTER=J92 DEVMLB SYNC DATE=06/28/2013

PAGE TITLE
Chipset Support

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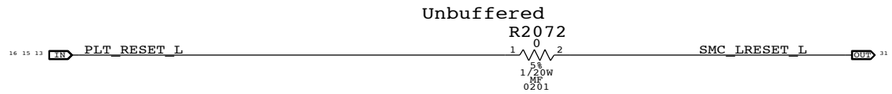
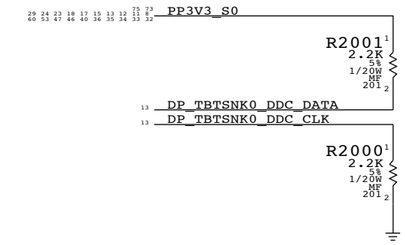
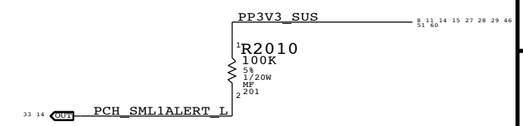
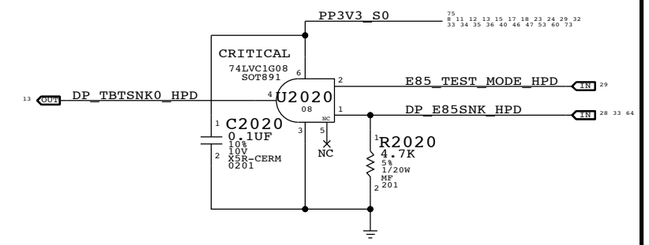
Platform Reset Connections



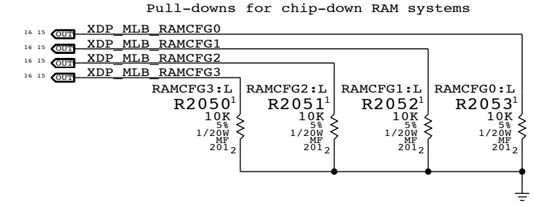




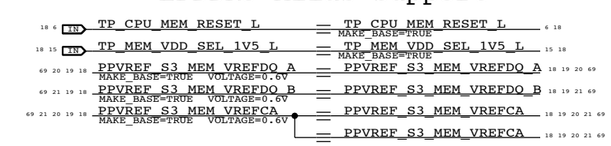


RAM Configuration Straps

Pull-downs for chip-down RAM systems



LPDDR3 Alias Support



SYNC MASTER=J92 DEVMLB SYNC DATE=08/01/2013

PAGE TITLE
Project Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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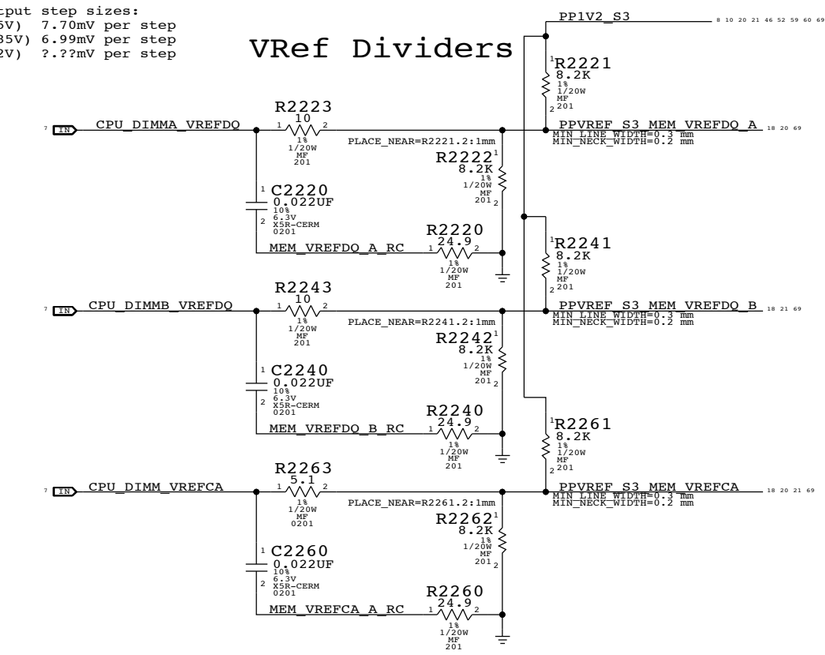
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



SYNC MASTER=J92 DEVMLB SYNC DATE=06/28/2013

PAGE TITLE
LPDDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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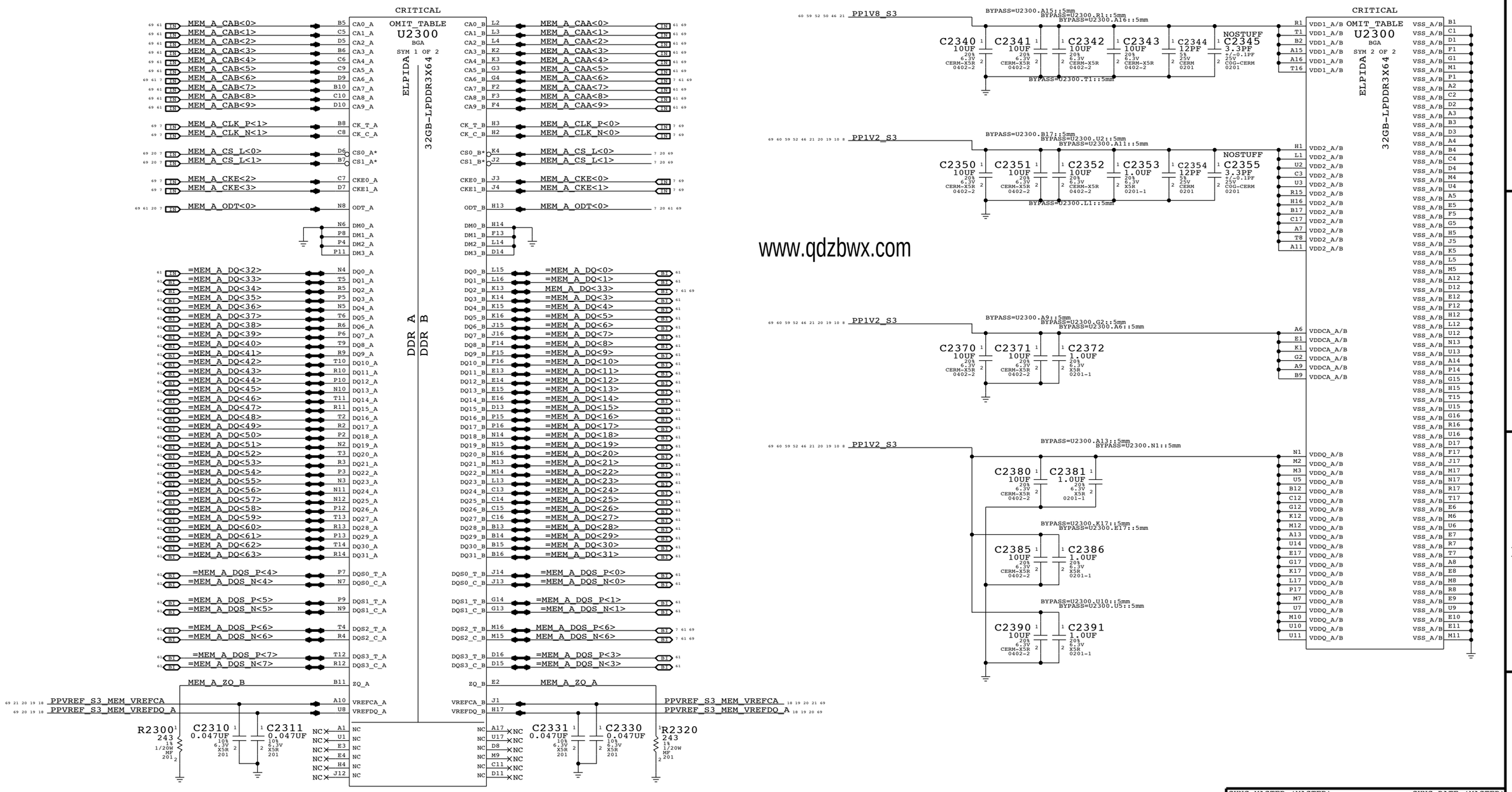

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SYNC MASTER=(MASTER) SYNC DATE=(MASTER)

PAGE TITLE

LPDDR3 DRAM Channel A (0-63)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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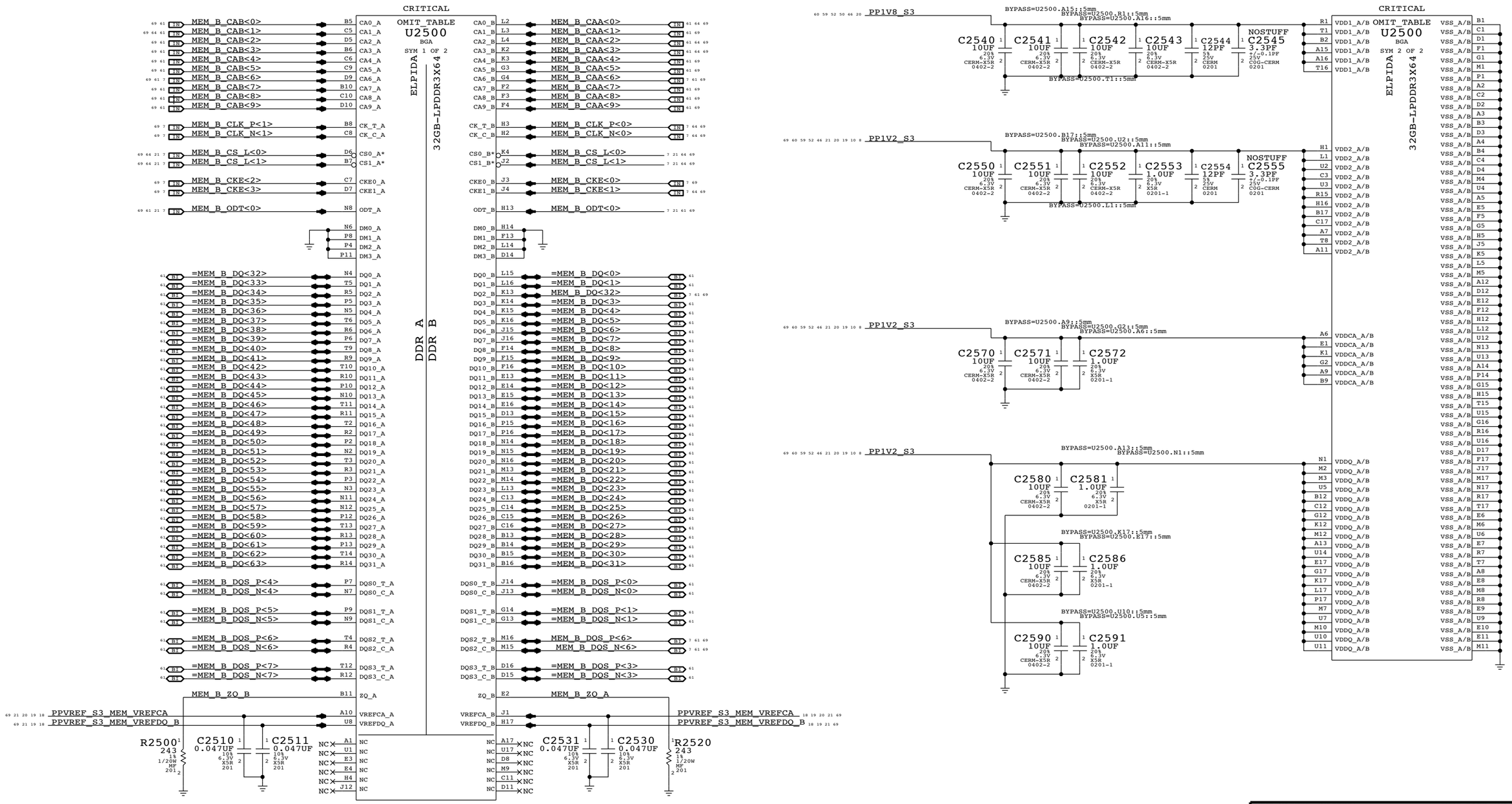

SYNC MASTER=(MASTER) SYNC DATE=(MASTER)

PAGE TITLE

LPDDR3 DRAM Channel B (0-63)

Apple Inc.

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REVISION <E4LABEL>

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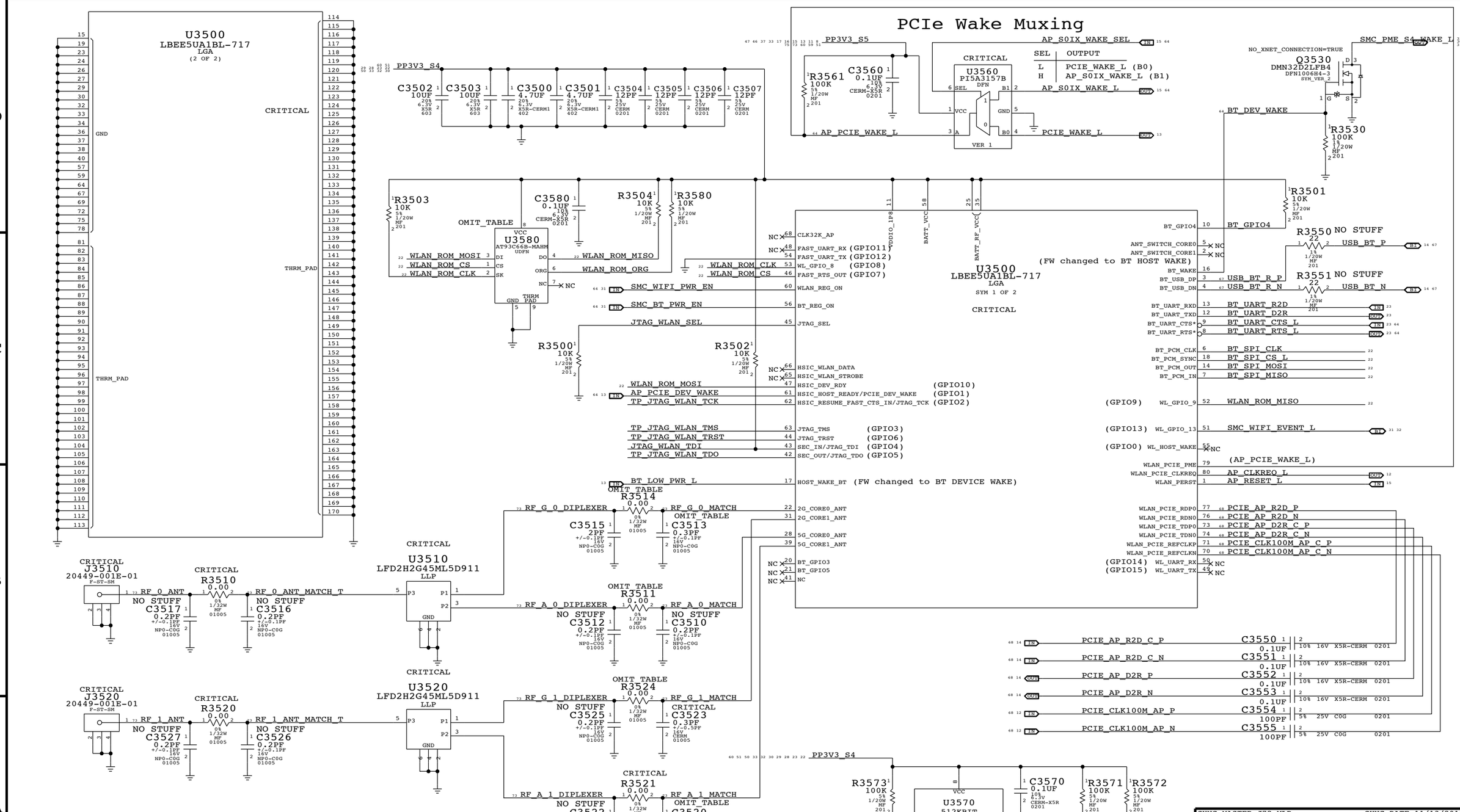

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S0259	1	CAP,7PF,+/-0.1PF,16V,01005	R3514	CRITICAL	
152S1742	1	IND,FILM,1.6NH,+/-0.1NH,200MA,01005	C3513	CRITICAL	
152S1544	1	IND,FILM,0.4NH,+/-0.1NH,270MA,01005	R3511	CRITICAL	
152S1564	1	IND,FILM,2.4NH,+/-0.1NH,200MA,01005	R3524	CRITICAL	
152S1720	1	IND,FILM,1.8NH,+/-0.1NH,270MA,01005	C3520	CRITICAL	

SYNC MASTER=J72 MLB SYNC DATE=11/13/2012

PAGE TITLE
WIFI/BT: MODULE

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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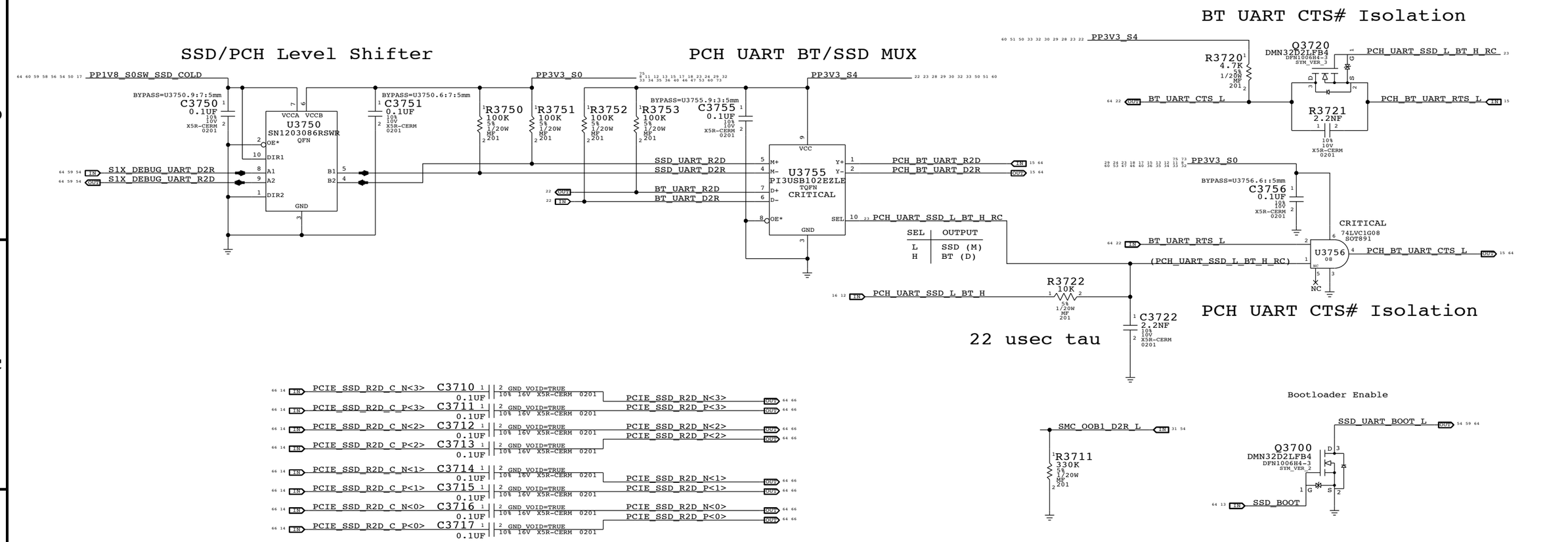

SYNC MASTER=J92 DEVMLB	SYNC DATE=09/11/2013
PAGE TITLE: SSD Support	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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	PAGE: 37 OF 130
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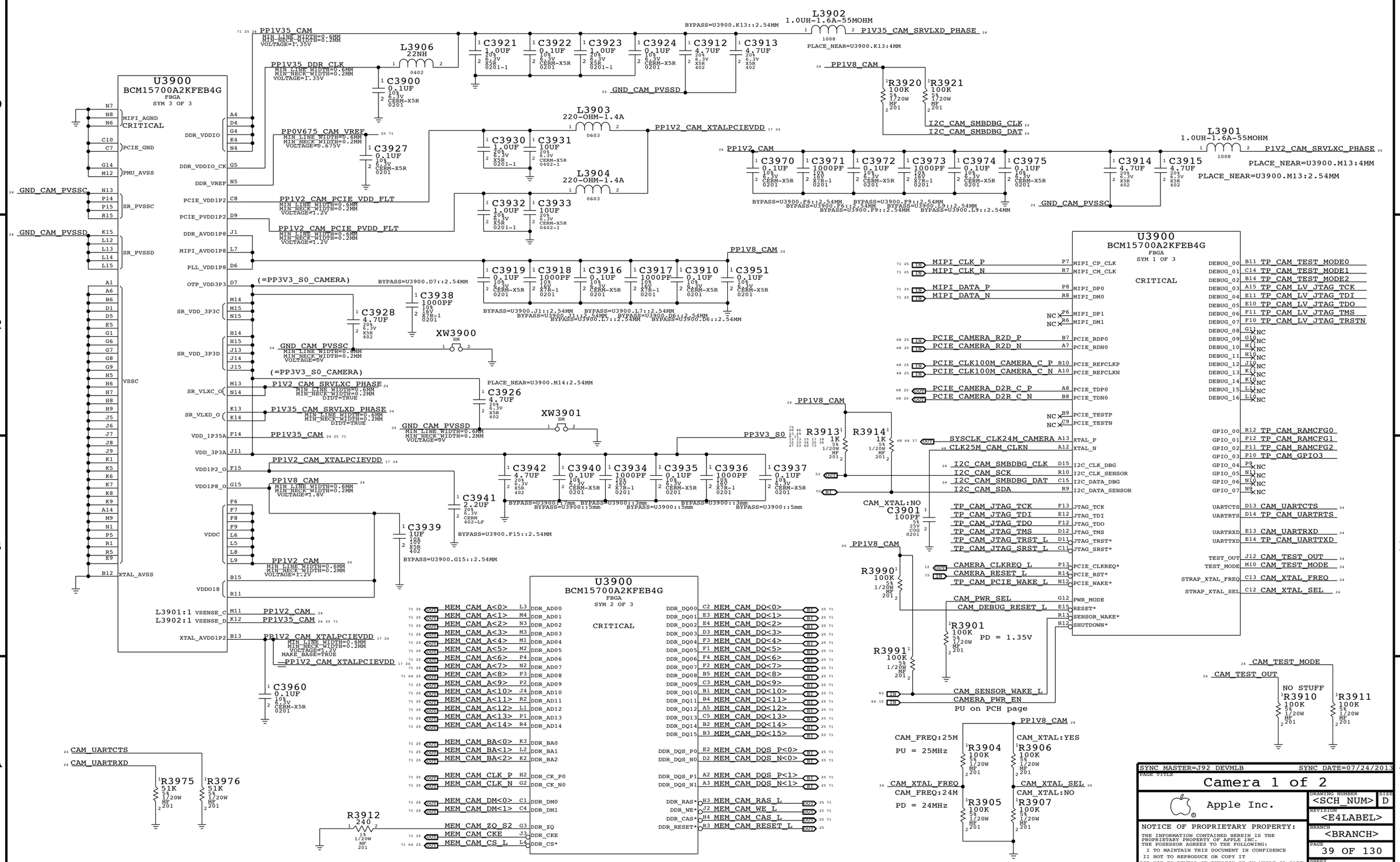
U3900
BCM15700A2KFEB4G
FBGA
SYM 3 OF 3
U3900
BCM15700A2KFEB4G
FBGA
SYM 1 OF 3
CRITICAL
U3900
BCM15700A2KFEB4G
FBGA
SYM 2 OF 3
CRITICAL
L3902
1.0UH-1.6A-55MOHM
P1V35_CAM_SRVLXD_PHASE
L3901
1.0UH-1.6A-55MOHM
P1V2_CAM_SRVLXC_PHASE
PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M13:2.54MM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP1V2_CAM_XTALPCIEVDD
PP1V8_CAM
PP1V2_CAM
GND_CAM_PVSSD
GND_CAM_PVSSC
(=PP3V3_S0_CAMERA)
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP3V3_S0
XW3900
XW3901
I2C_CAM_SMBDBG_CLK
I2C_CAM_SMBDBG_DAT
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
SYSCLK_CLK24M_CAMERA
CLK25M_CAM_CLKN
I2C_CAM_SCK
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
TP_CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAMERA_RESET_L
TP_CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
PU on PCH page
CAM_XTAL:NO
CAM_FREQ:25M
PU = 25MHz
CAM_FREQ:24M
PD = 24MHz
CAM_XTAL:YES
CAM_XTAL_FREQ
CAM_XTAL_SEL
CAM_XTAL:NO
PD = 1.35V
CAM_TEST_MODE
CAM_TEST_OUT
NO STUFF
CAM_UARTCTS
CAM_UARTRXD
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
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MEM_CAM_CLK_P
MEM_CAM_CLK_N
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MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
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MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
TP_CAM_TEST_MODE0
TP_CAM_TEST_MODE1
TP_CAM_TEST_MODE2
TP_CAM_LV_JTAG_TCK
TP_CAM_LV_JTAG_TDI
TP_CAM_LV_JTAG_TDO
TP_CAM_LV_JTAG_TMS
TP_CAM_LV_JTAG_TRSTN
TP_CAM_RAMCFG0
TP_CAM_RAMCFG1
TP_CAM_RAMCFG2
TP_CAM_GPIO3
CAM_UARTCTS
CAM_UARTRTS
CAM_UARTRXD
TP_CAM_UARTTXD
CAM_TEST_OUT
CAM_TEST_MODE
CAM_XTAL_FREQ
CAM_XTAL_SEL
SYNC MASTER=J92 DEVMLB
SYNC DATE=07/24/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
BRANCH
<BRANCH>
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39 OF 130
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24 OF 75
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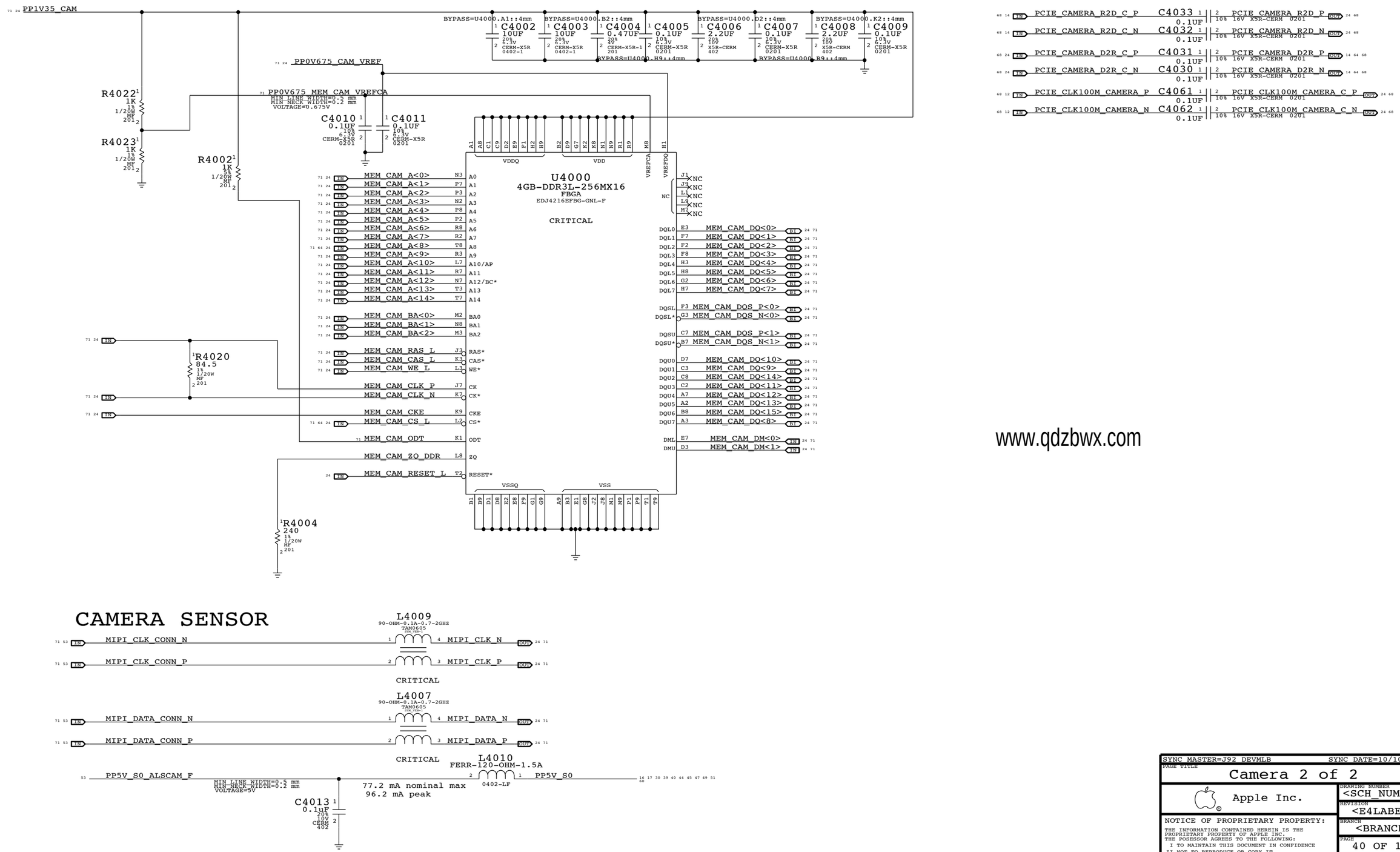

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SYNC MASTER=J92 DEVMLB SYNC DATE=10/10/2013

PAGE TITLE
Camera 2 of 2

Apple Inc.

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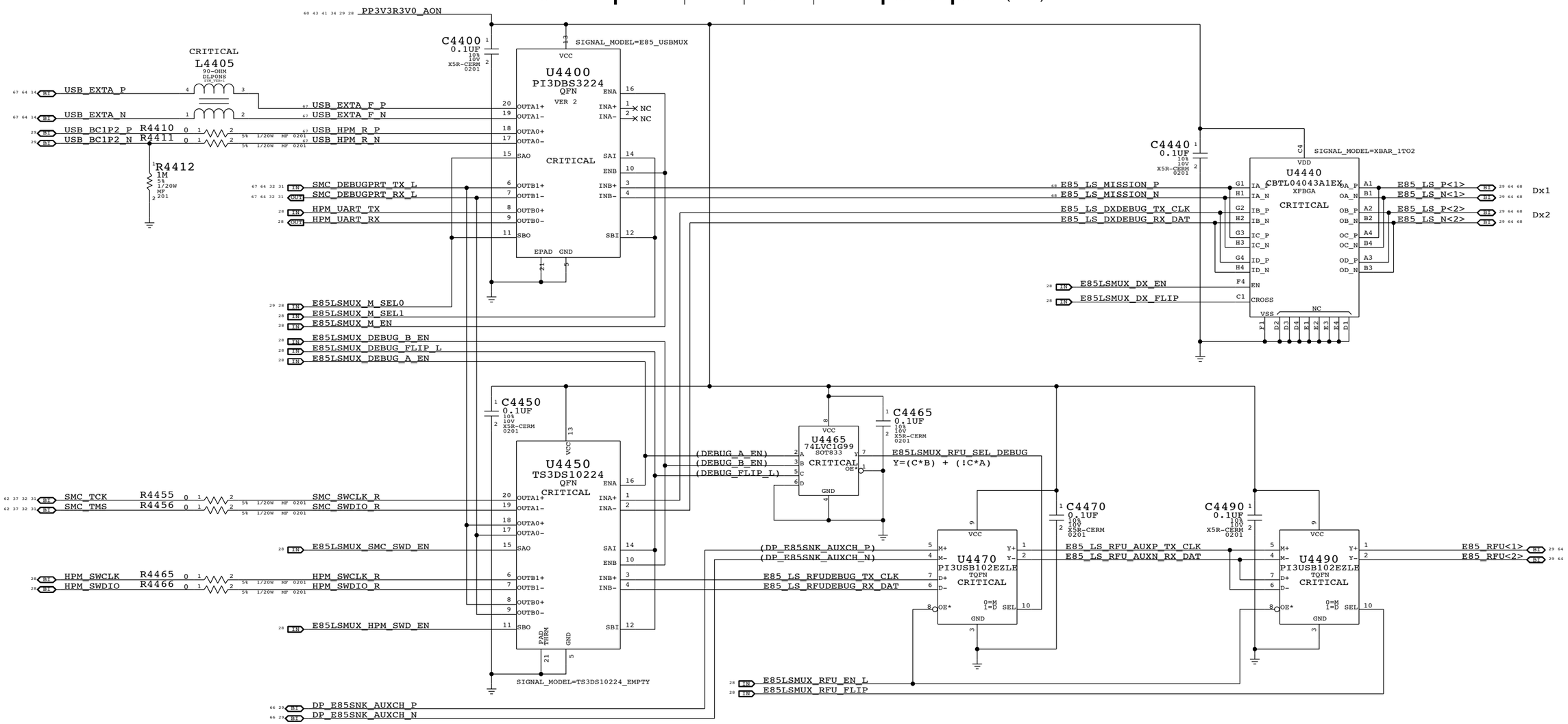
Mode	DX_EN	M_EN	M_SEL0	M_SEL1	INB	Mission
Empty	0	0	X	X	Hi-Z	Hi-Z
Mojo	1	1	1	1	OUTB1	UART (SMC)
USB (Host)	1	1	1	0	OUTA1	USB (PCH)
USB (Device)	1	1	0	0	OUTA0	USB (HPM)
HPM UART	1	1	0	1	OUTB0	UART (HPM)



Mode	DX_EN	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INA	DXDEBUG
Empty	0	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
No Debug	1	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
SMC SWD	1	1	X	1	1	X	OUTA1	SWD (SMC)
Mojo	1	1 X	X 1	1 0	0 X	X 0	OUTA0 OUTB0	UART (SMC)
HPM SWD	1	X	1	0	X	1	OUTB1	SWD (HPM)

Mode	RFU_EN_L	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INB	RFU
Empty	1	X 0	0 X	1 0	X	X	Hi-Z	Hi-Z
DP	0	X 0	0 X	1 0	X	X	Hi-Z	AUX+/HPD
HPM SWD	0	X	1	1	X	1	OUTB1	SWD (HPM)
Mojo	0	X 1	1 X	1 0	X 0	0 X	OUTB0 OUTA0	UART (SMC)
SMC SWD	0	1	X	0	1	X	OUTA1	SWD (SMC)

SYNC MASTER=J92 DEVMLB SYNC DATE=07/08/2014

PAGE TITLE
Low Speed MUXing

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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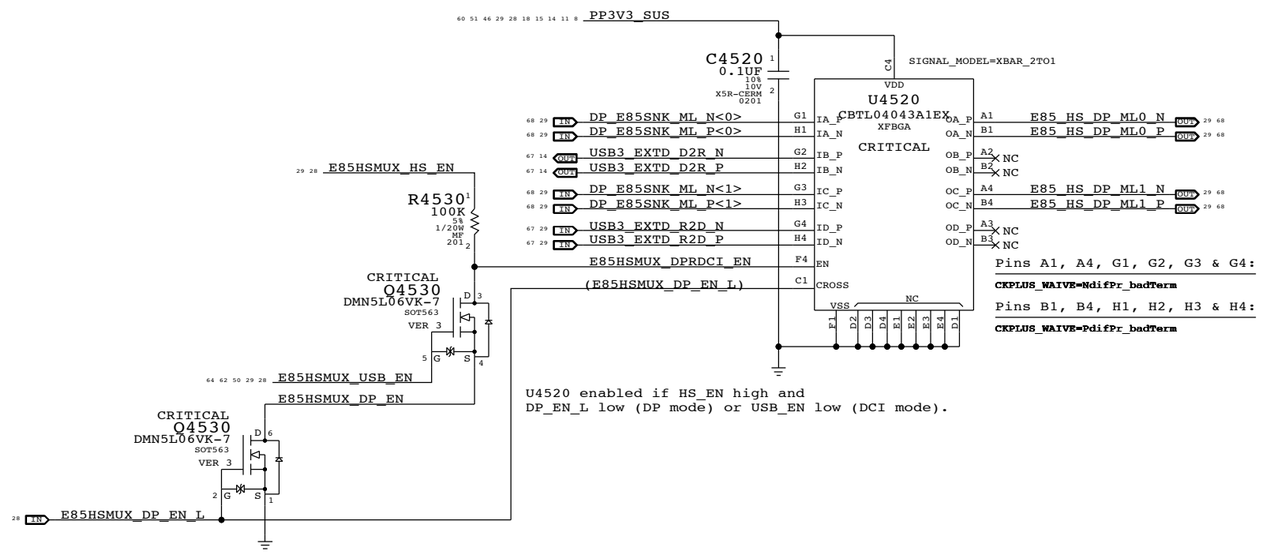

HS_FLIP swaps Tx1/2 and Rx1/2

Mode	HS_EN	DP_EN_L	USB_EN	SSTx1	SSRx1	SSTx2	SSRx2
Empty	0	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
USB3	1	1	1	R2D	D2R	Hi-Z	Hi-Z
USB3/DPx2	1	0	1	R2D	D2R	ML1	ML0
DPx4 (Passive)	1	0	0	ML2	ML3	ML1	ML0
DCI (Debug)	1	1	0	(ML2)	(ML3)	DCI-R2D	DCI-D2R

NOTE: Invert HS_FLIP in DCI mode to put DCI-USB on USB3 pins. USB3 and DP not usable in DCI mode.

SYNC MASTER=DEV_MLB SYNC DATE=04/17/2014

PAGE TITLE
High Speed MUXing

Apple Inc.

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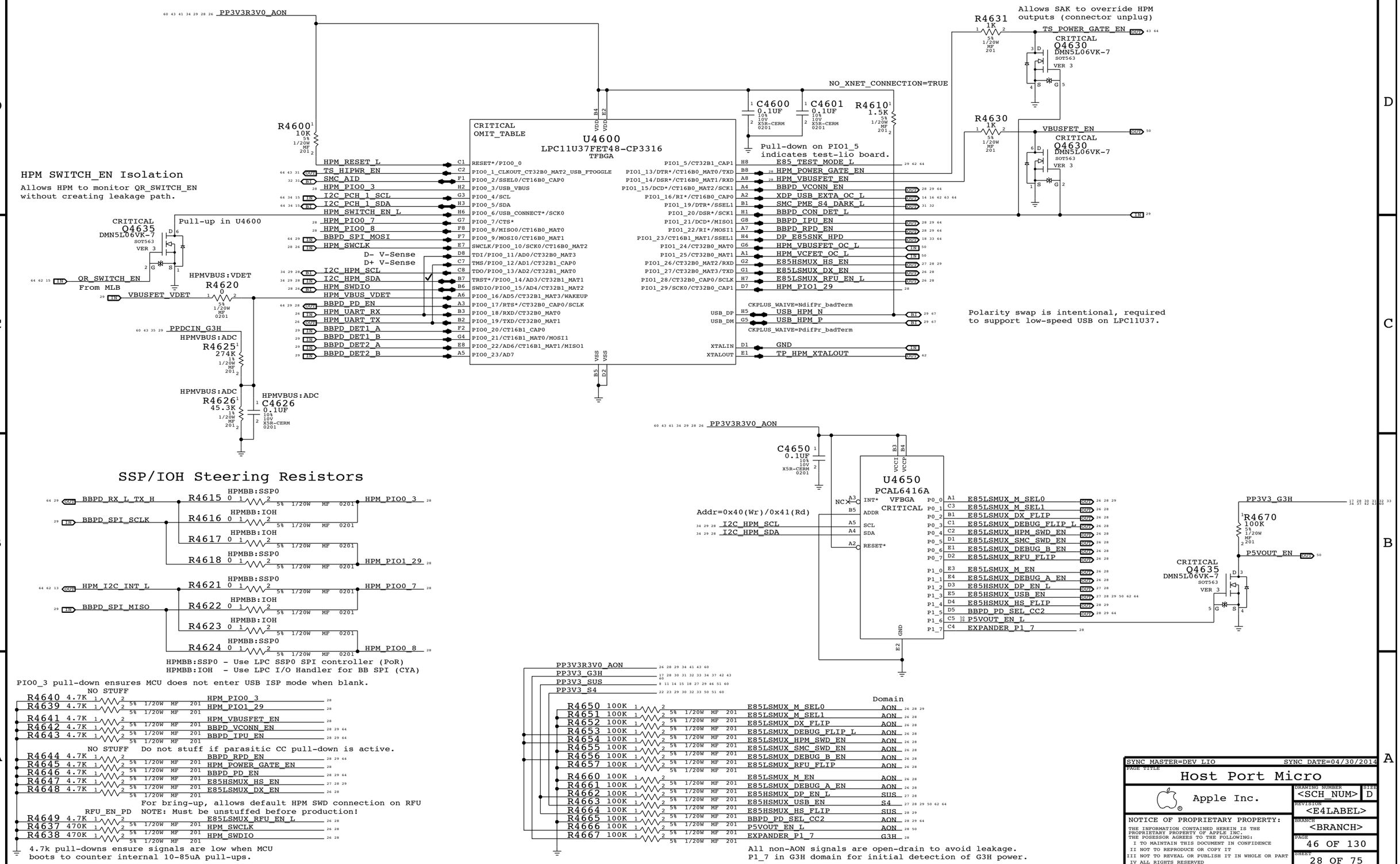

SYNC MASTER=DEV LIO SYNC DATE=04/30/2014

PAGE TITLE

Host Port Micro

Apple Inc.

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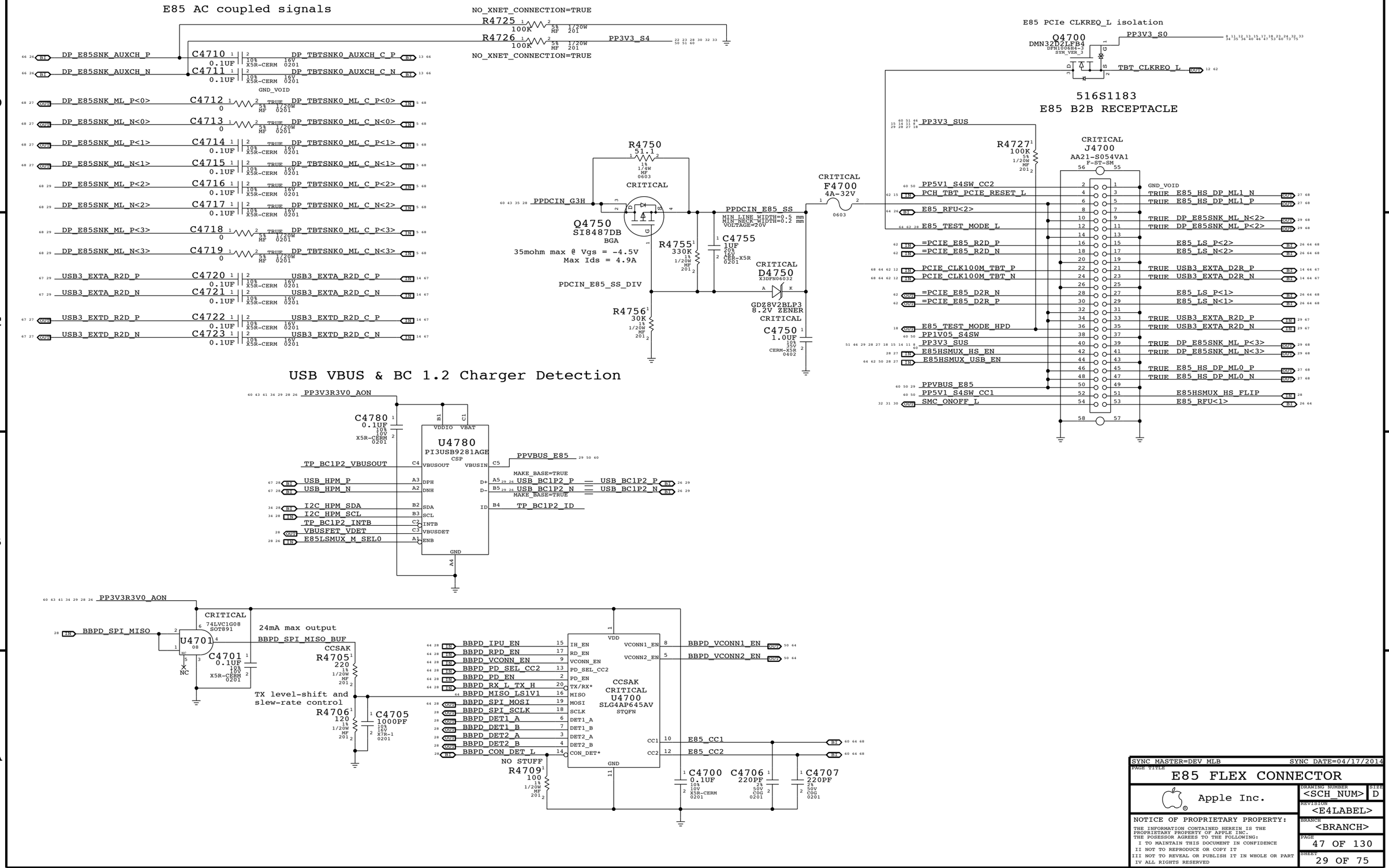

SYNC MASTER=DEV_MLB SYNC DATE=04/17/2014

PAGE TITLE

E85 FLEX CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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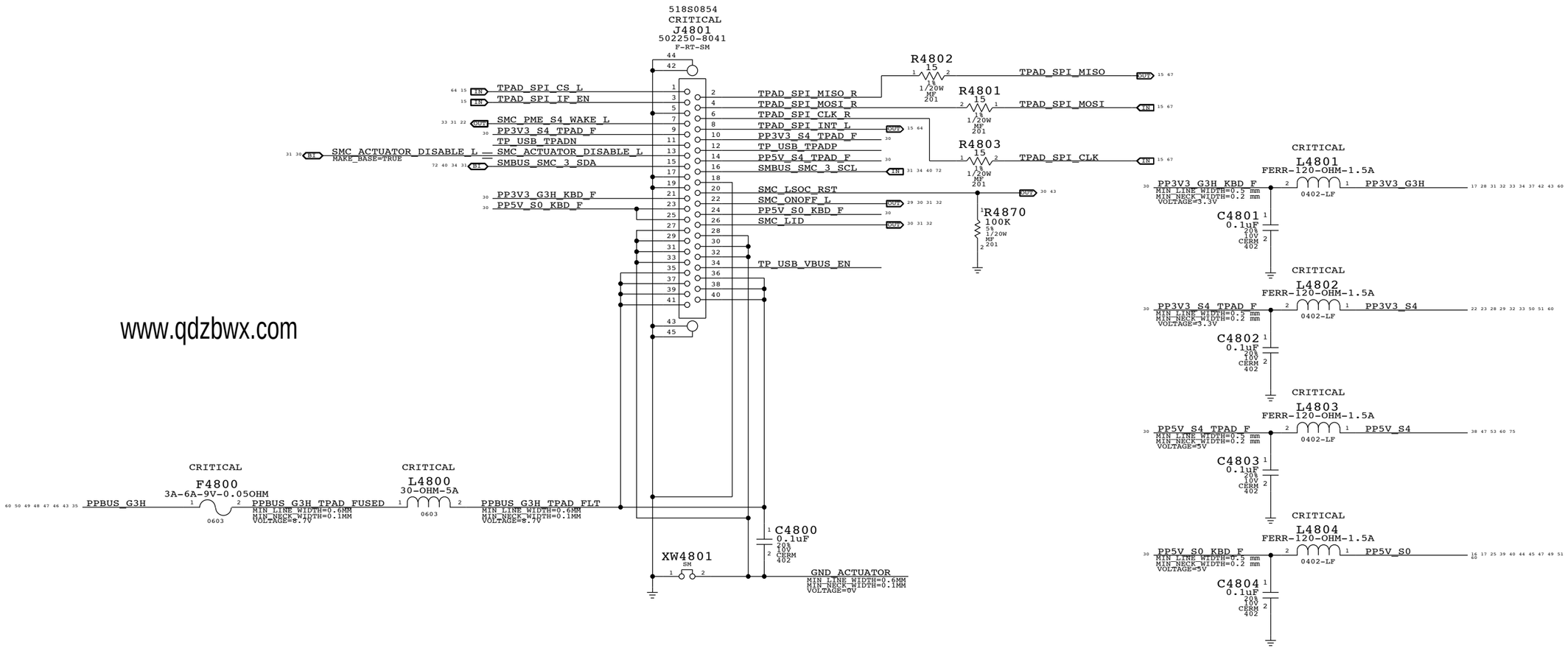
IPD ZIF CONNECTOR

Bottom side contacts used
Pinout reversed from flex



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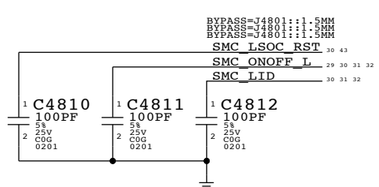

SYNC MASTER=J92 DEVMLB SYNC DATE=03/26/2014

PAGE TITLE
Keyboard & Trackpad Conn

Apple Inc.

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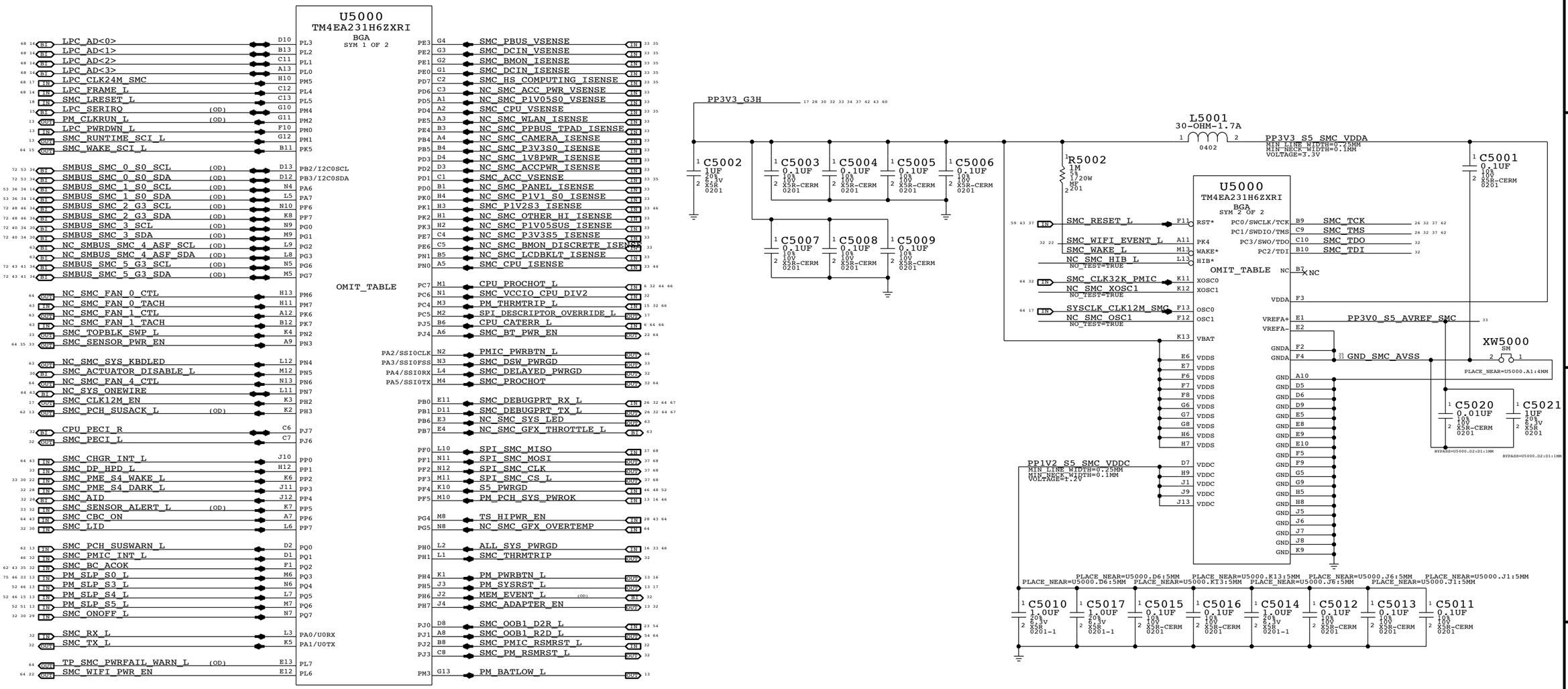

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=J92 DEVMLB SYNC DATE=10/11/2013

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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PAGE TITLE

SMC Shared Support

Apple Inc.

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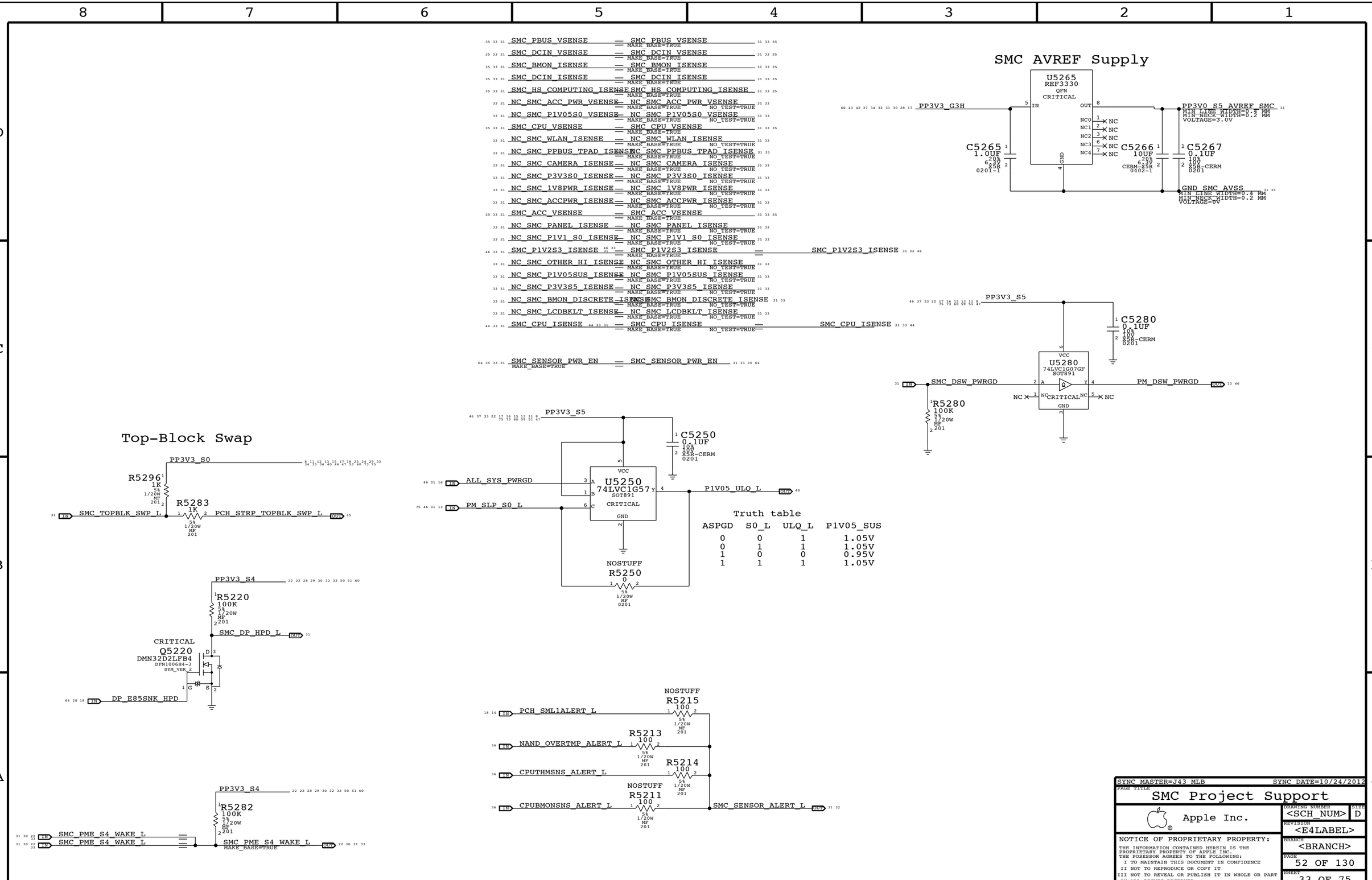
SMC_PBUS_VSENSE — SMC_PBUS_VSENSE
SMC_DCIN_VSENSE — SMC_DCIN_VSENSE
SMC_BMON_ISENSE — SMC_BMON_ISENSE
SMC_DCIN_ISENSE — SMC_DCIN_ISENSE
SMC_HS_COMPUTING_ISENSE — SMC_HS_COMPUTING_ISENSE
NC_SMC_ACC_PWR_VSENSE — NC_SMC_ACC_PWR_VSENSE
NC_SMC_P1V05S0_VSENSE — NC_SMC_P1V05S0_VSENSE
SMC_CPU_VSENSE — SMC_CPU_VSENSE
NC_SMC_WLAN_ISENSE — NC_SMC_WLAN_ISENSE
NC_SMC_PPBUS_TPAD_ISENSE — NC_SMC_PPBUS_TPAD_ISENSE
NC_SMC_CAMERA_ISENSE — NC_SMC_CAMERA_ISENSE
NC_SMC_P3V3S0_ISENSE — NC_SMC_P3V3S0_ISENSE
NC_SMC_1V8PWR_ISENSE — NC_SMC_1V8PWR_ISENSE
NC_SMC_ACCPWR_ISENSE — NC_SMC_ACCPWR_ISENSE
SMC_ACC_VSENSE — SMC_ACC_VSENSE
NC_SMC_PANEL_ISENSE — NC_SMC_PANEL_ISENSE
NC_SMC_P1V1_S0_ISENSE — NC_SMC_P1V1_S0_ISENSE
SMC_P1V2S3_ISENSE — SMC_P1V2S3_ISENSE
NC_SMC_OTHER_HI_ISENSE — NC_SMC_OTHER_HI_ISENSE
NC_SMC_P1V05SUS_ISENSE — NC_SMC_P1V05SUS_ISENSE
NC_SMC_P3V3S5_ISENSE — NC_SMC_P3V3S5_ISENSE
NC_SMC_BMON_DISCRETE_ISENSE — NC_SMC_BMON_DISCRETE_ISENSE
NC_SMC_LCDBKLT_ISENSE — NC_SMC_LCDBKLT_ISENSE
SMC_CPU_ISENSE — SMC_CPU_ISENSE
SMC_SENSOR_PWR_EN — SMC_SENSOR_PWR_EN
MAKE_BASE=TRUE
NO_TEST=TRUE
SMC AVREF Supply
U5265
REF3330
QFN
CRITICAL
PP3V3_G3H
IN
OUT
GND
NC0
NC1
NC2
NC3
NC4
NC
C5265
1.0UF
20%
6.3V
X5R
0201-1
C5266
10UF
20%
6.3V
CERM-X5R
0402-1
C5267
0.1UF
10%
10V
X5R-CERM
0201
PP3V0_S5_AVREF_SMC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.0V
GND_SMC_AVSS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
PP3V3_S5
C5280
0.1UF
10%
10V
X5R-CERM
0201
VCC
U5280
74LVC1G07GF
SOT891
SMC_DSW_PWRGD
PM_DSW_PWRGD
CRITICAL
R5280
100K
5%
1/20W
MF
201
PP3V3_S5
C5250
0.1UF
10%
10V
X5R-CERM
0201
VCC
U5250
74LVC1G57
SOT891
CRITICAL
GND
ALL_SYS_PWRGD
PM_SLP_S0_L
P1V05_ULQ_L
NOSTUFF
R5250
0
5%
1/20W
MF
0201
Truth table
ASPGD S0_L ULQ_L P1V05_SUS
0 0 1 1.05V
0 1 1 1.05V
1 0 0 0.95V
1 1 1 1.05V
Top-Block Swap
PP3V3_S0
R5296
1K
5%
1/20W
MF
201
R5283
1K
5%
1/20W
MF
201
SMC_TOPBLK_SWP_L
PCH_STRP_TOPBLK_SWP_L
PP3V3_S4
R5220
100K
5%
1/20W
MF
201
SMC_DP_HPD_L
CRITICAL
Q5220
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
DP_E85SNK_HPD
NOSTUFF
R5215
100
5%
1/20W
MF
201
PCH_SML1ALERT_L
R5213
100
5%
1/20W
MF
201
NAND_OVERTMP_ALERT_L
R5214
100
5%
1/20W
MF
201
CPUTHMSNS_ALERT_L
NOSTUFF
R5211
100
5%
1/20W
MF
201
CPUBMONSNS_ALERT_L
SMC_SENSOR_ALERT_L
PP3V3_S4
R5282
100K
5%
1/20W
MF
201
SMC_PME_S4_WAKE_L
SMC_PME_S4_WAKE_L
MAKE_BASE=TRUE
SYNC_MASTER=J43_MLB
SYNC_DATE=10/24/2012
PAGE TITLE
SMC Project Support
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
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<BRANCH>
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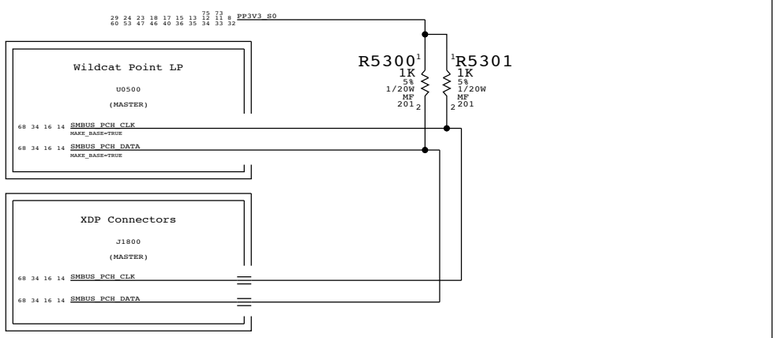
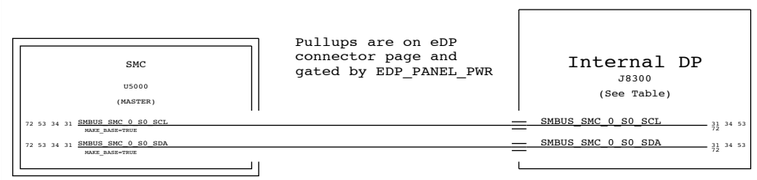
Wildcat Point LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

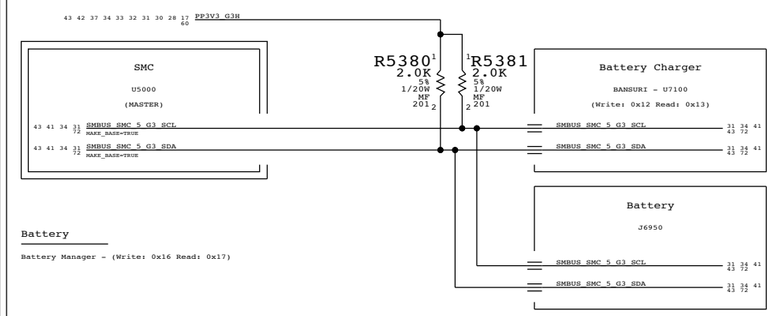


(* = Multiple options)

Internal DP

	J43		J41		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

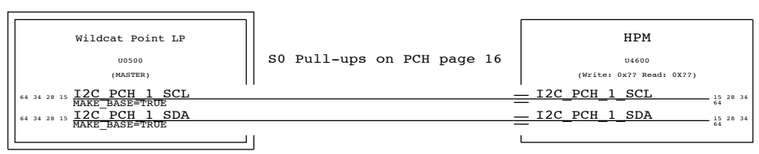
SMC "5" SMBus G3H Connections



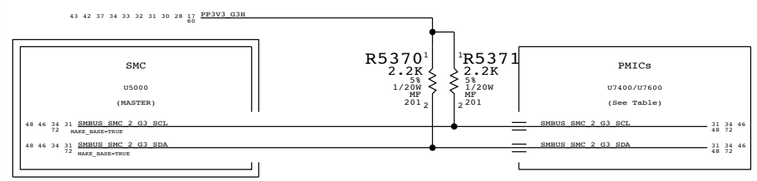
Battery

Battery Manager - (Write: 0x16 Read: 0x17)

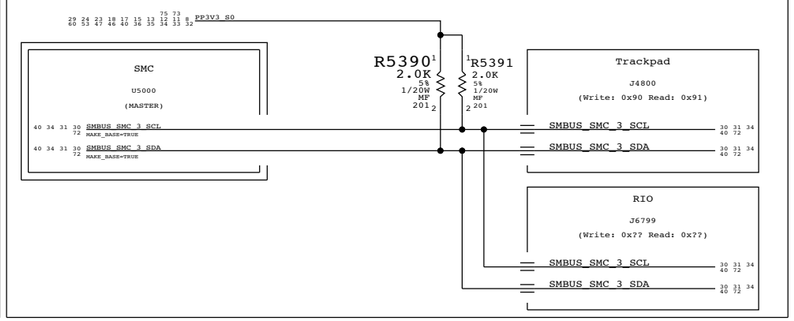
Wildcat Point LP S0 I2C "1" Connections



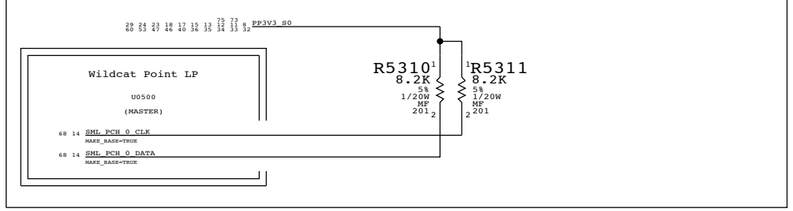
SMC "2" SMBus S3 Connections



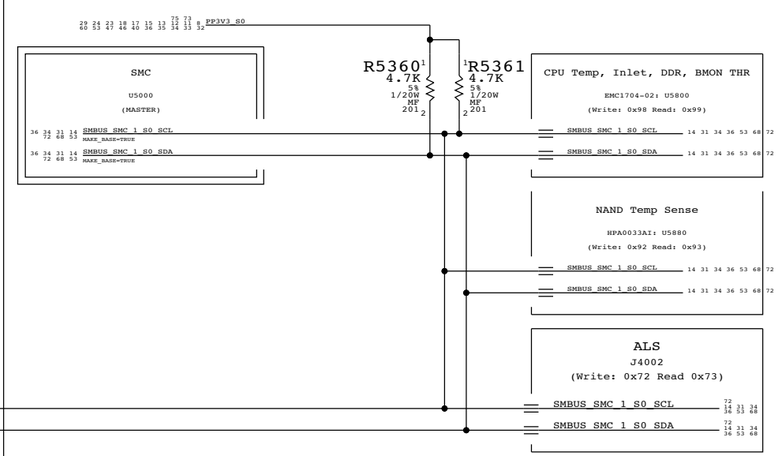
SMC "3" SMBus S0 Connections



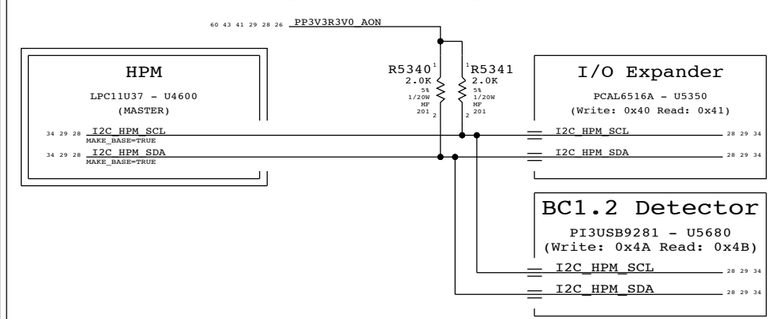
Wildcat Point LP S0 "SMLink 0" Connections



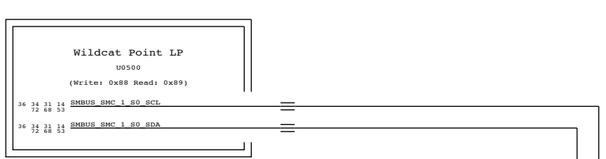
SMC S0 "1" SMBus Connections



HPM Master Bus



Wildcat Point LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH

SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE

SMBus Connections

Apple Inc.

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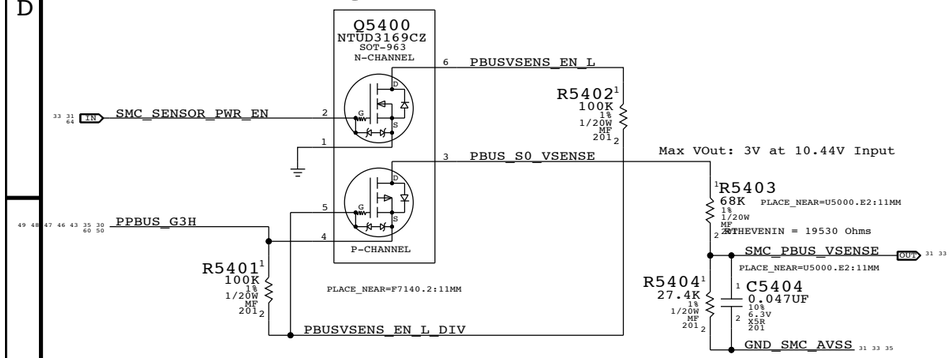
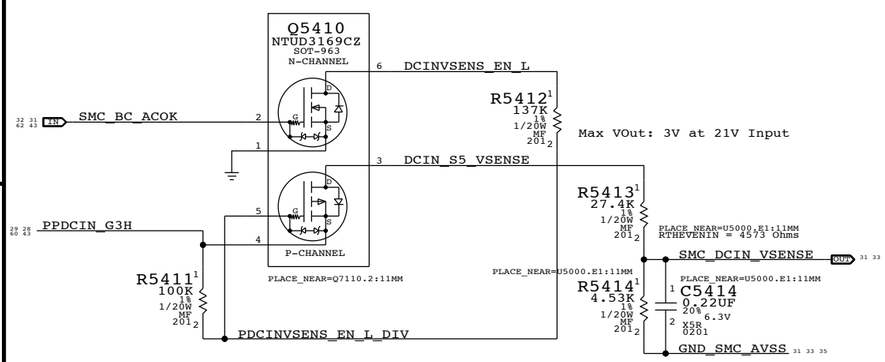
POR VOLTAGE / CURRENT SENSORS : TO BE USED IN PRODUCTION

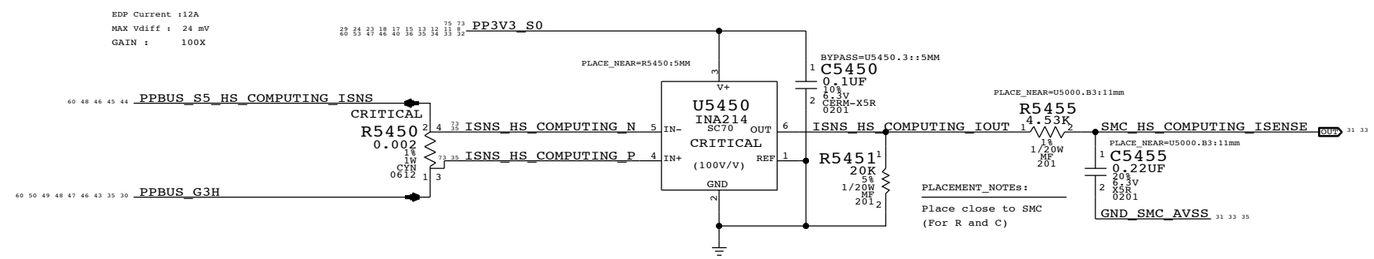
VP0R: PBUS Voltage Sense Enable & Filter



VD0R: DC-In Voltage Sense Enable & Filter

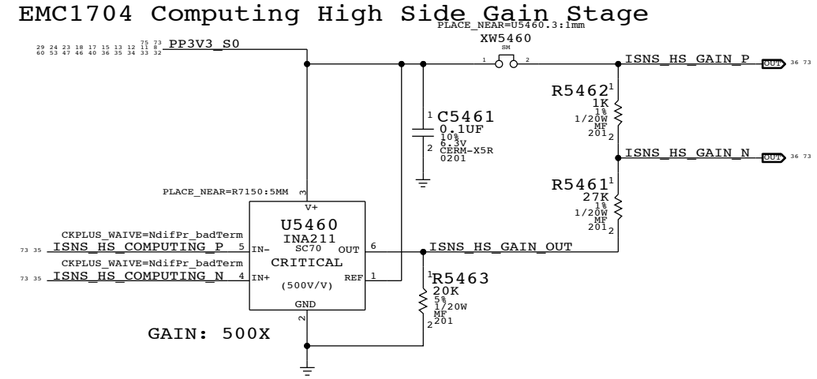


IC0R : COMPUTING High Side Current Sense



Need to set gains for ULX

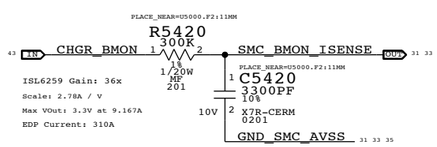
EMC1704 Computing High Side Gain Stage



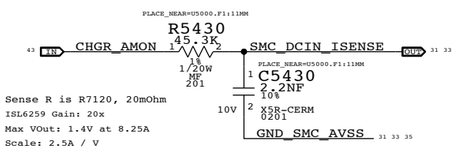
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

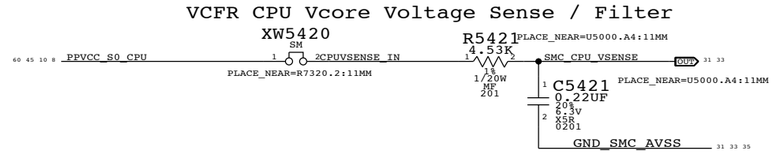
CHARGER BMON High Side Current Sense



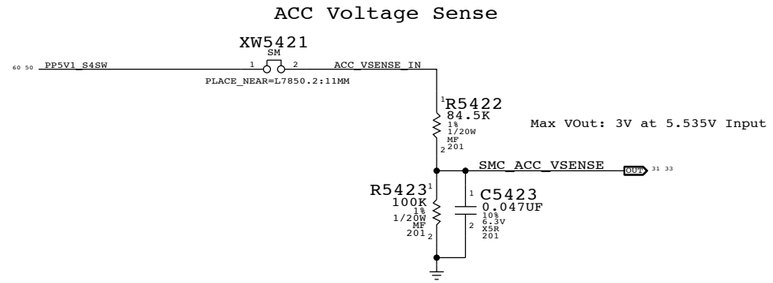
DC-IN (AMON) Current Sense



VCFR CPU Vcore Voltage Sense / Filter



ACC Voltage Sense



SYNC MASTER=J92_DEVMLB SYNC DATE=02/07/2014

PAGE TITLE: Voltage & Current Sensing

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REVISION: <E4LABEL>
BRANCH: <BRANCH>
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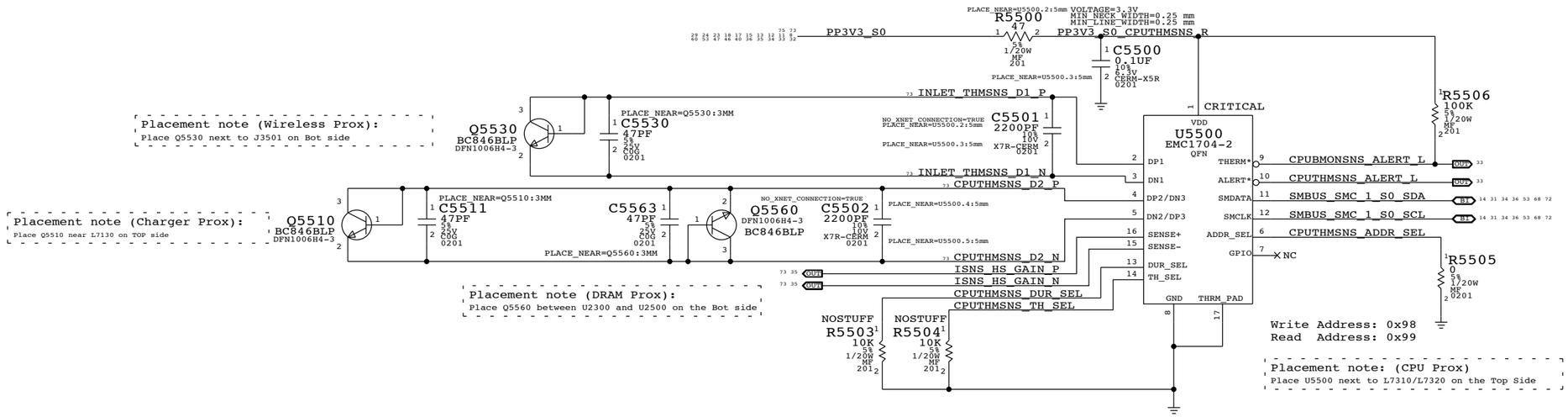
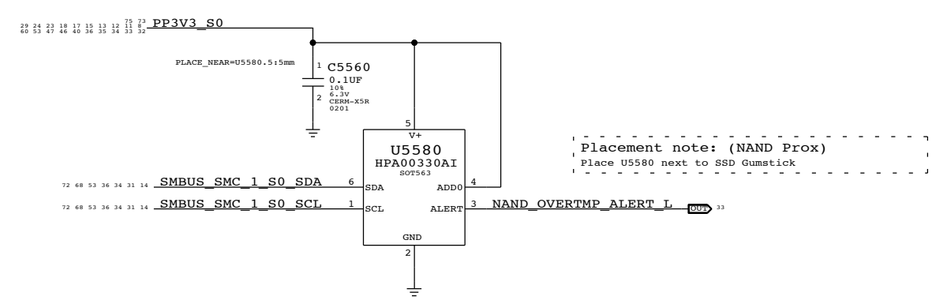
POR THERMAL SENSORS : TO BE USED IN PRODUCTION

CPU Proximity, Inlet ,DDR and BMON THR Sensor



NAND Temp Sensor



SYNC MASTER=J92 DEVMLB SYNC DATE=09/12/2013

PAGE TITLE
Temperature Sensing

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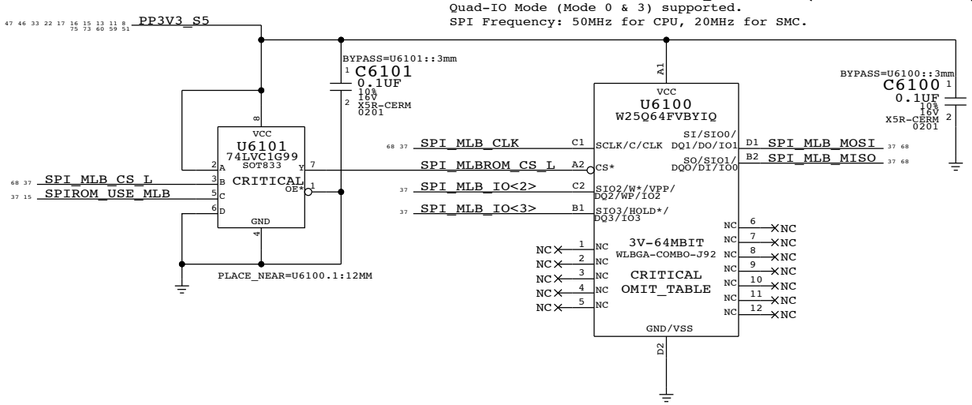
SPI ROM - Combo BGA Footprint (3 vendors)

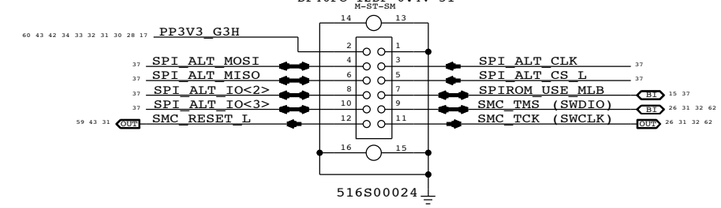
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



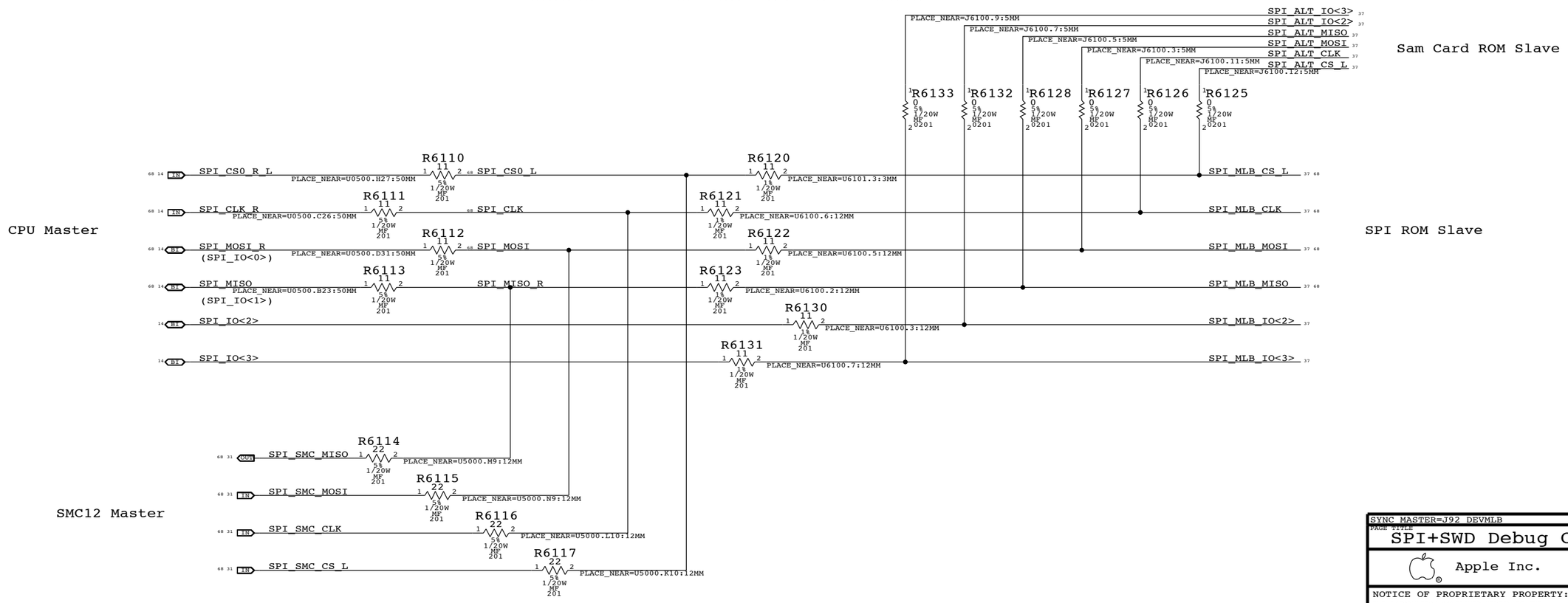
SPI+SWD SAM Connector

CRITICAL

J6100
DF40PC-12DP-0.4V-51
M-ST-SM



BootROM SPI Bus Series Termination



SYNC MASTER=J92 DEVMLB SYNC DATE=07/23/2013

PAGE TITLE
SPI+SWD Debug Connector

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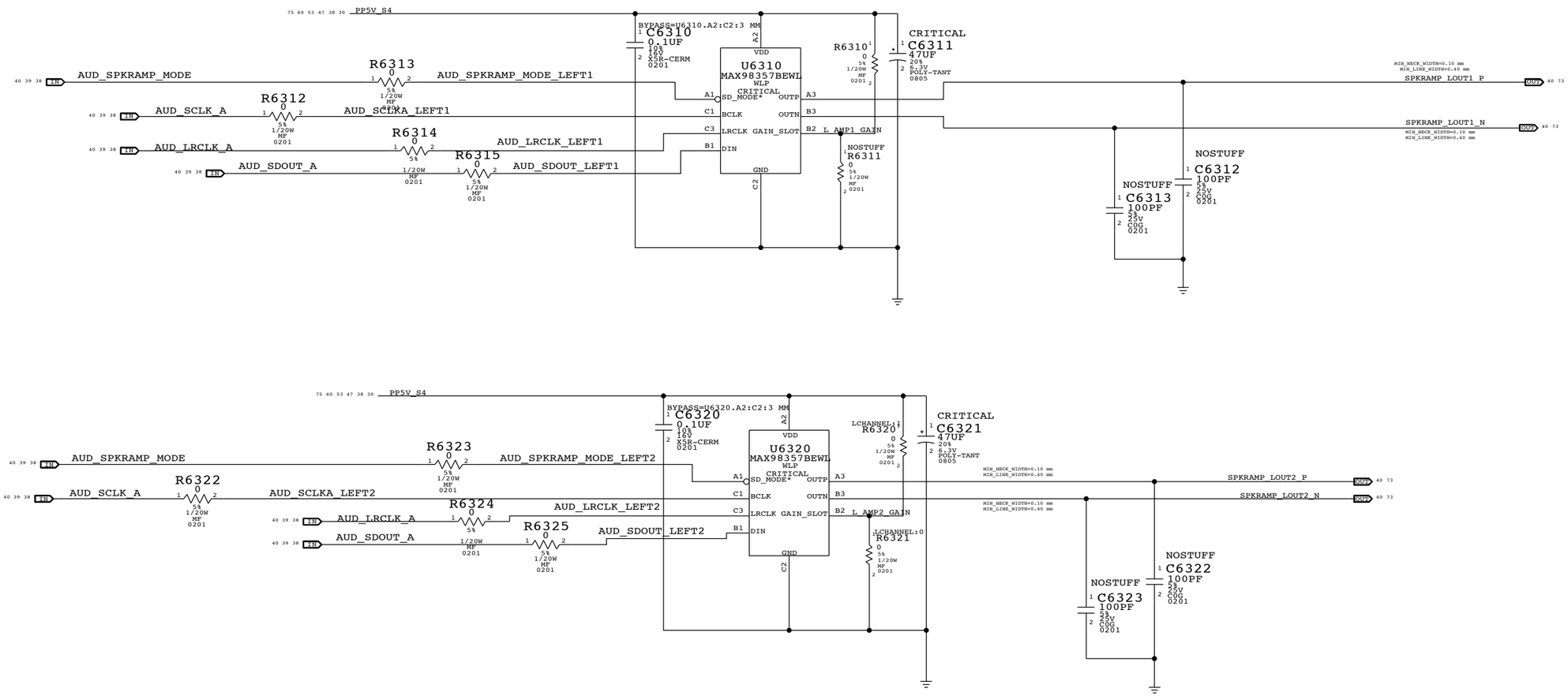
Left Speaker Amps

APPLE P/N 353S4265



SPEAKER CONFIGS

BOM GROUP	BOM OPTIONS
EQ:2CH	LCHANNEL:1,RCHANNEL:3
EQ:4CH	LCHANNEL:0,RCHANNEL:4

SYNC MASTER=J92 DEVMLB SYNC DATE=09/19/2013

PAGE TITLE
Audio:Left Speaker Amps

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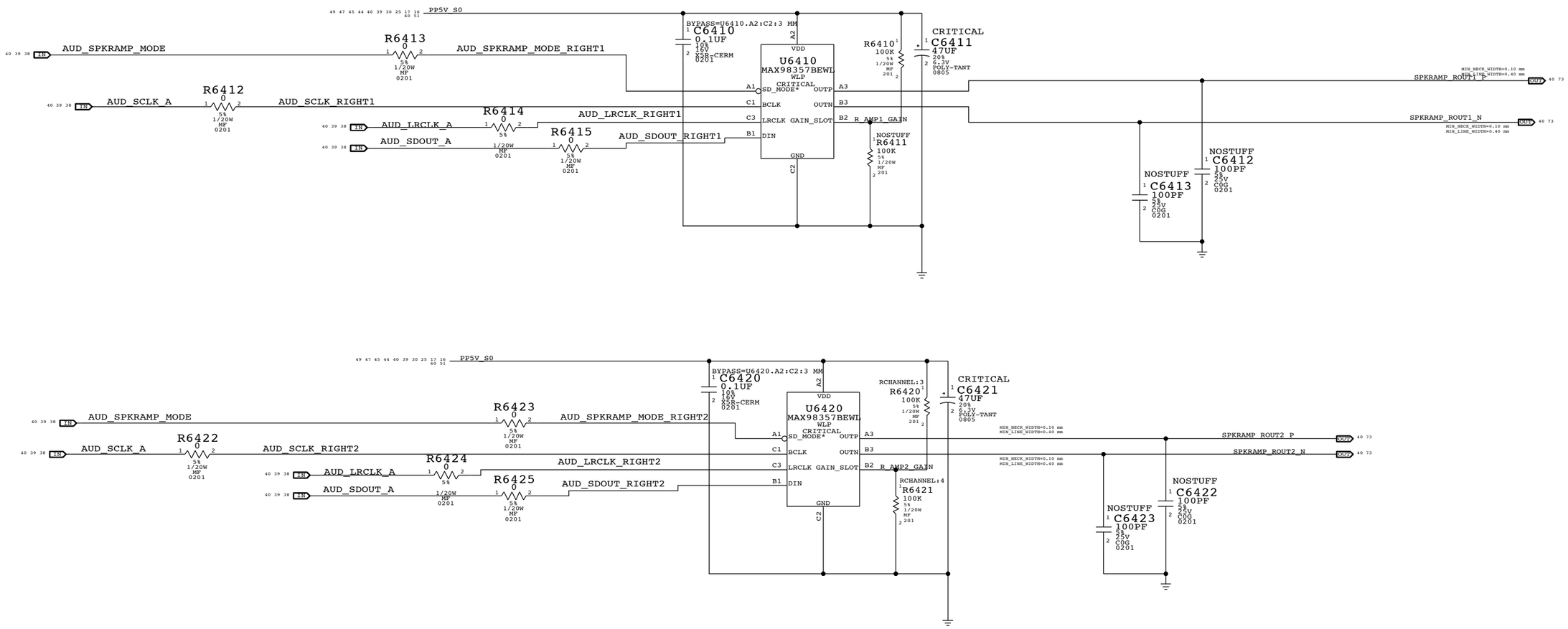
Right Speaker Amps

APPLE P/N 353S4265



SYNC MASTER=J92 DEVMLB SYNC DATE=09/19/2013

PAGE TITLE
Audio:Right Speaker Amps

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)		0X09 (A)
SPEAKERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A

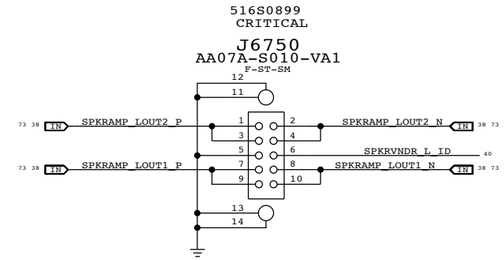
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

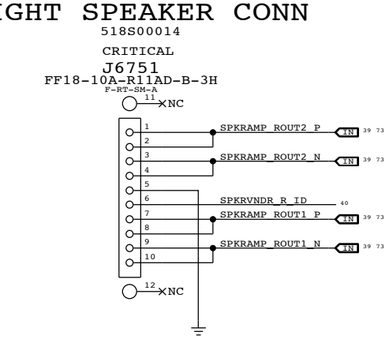
SOUTHBRIDGE RESOURCE/PIN ALLOCATIONS

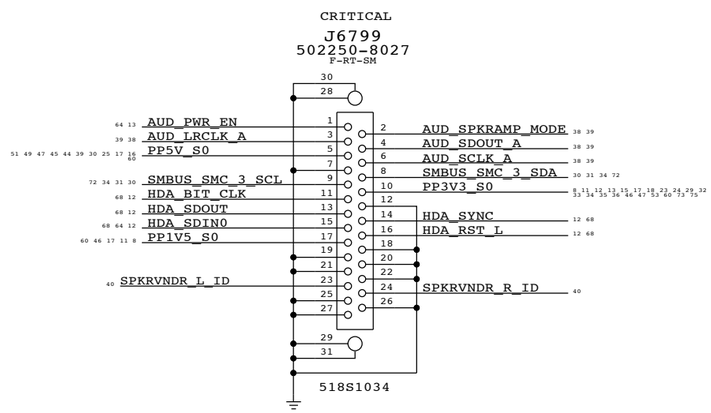
FUNCTION	NET NAME	SB GPIO/INT
PERIPHERAL/EXTRACTION DETECT	AUD_IP_PERIPHERAL_DET	GPIO 3
MIKEY INTERRUPT	AUD_I2C_INT_L	GPIO 5
MIKEY ENABLE	AUD_IPHS_SWITCH_EN	GPIO 16
MIKEY I2C BUS	I2C_MIKEY_SDA/SCL	PCH SMBUS 0

LEFT SPEAKER CONN



RIGHT SPEAKER CONN





RIO FLEX CONN

SYNC MASTER=CARA J92 SYNC DATE=04/17/2014

PAGE TITLE

AUDIO: CONNECTORS

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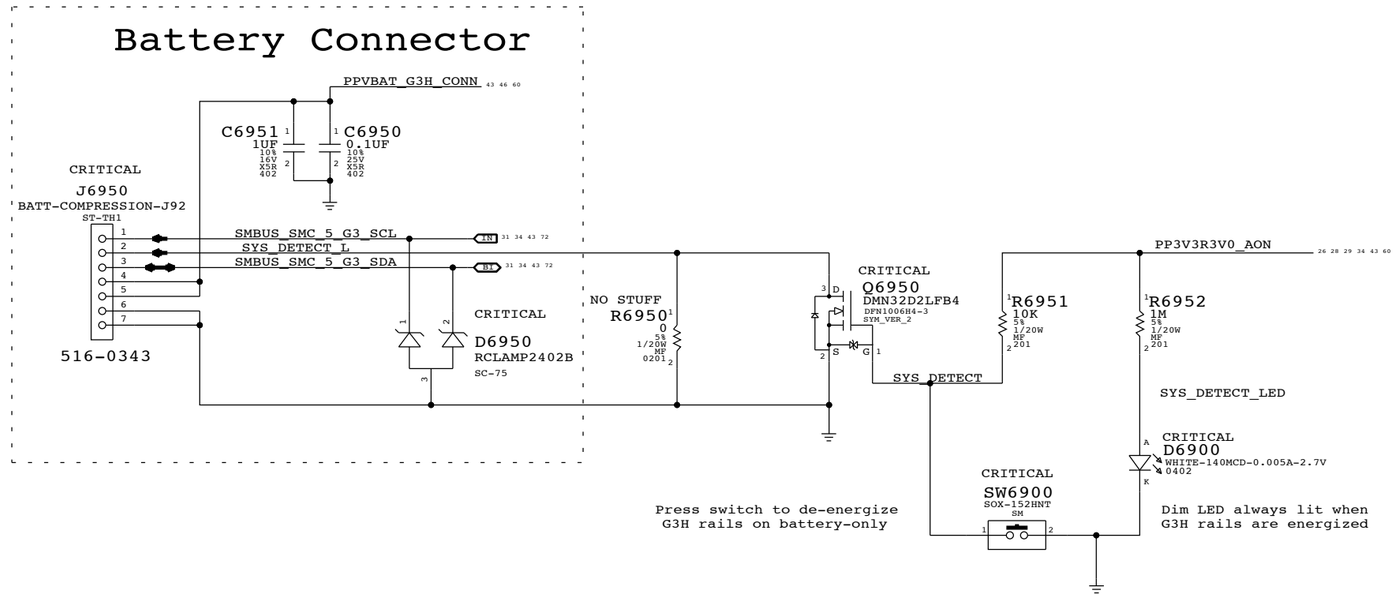
Battery Connector



SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE
Battery Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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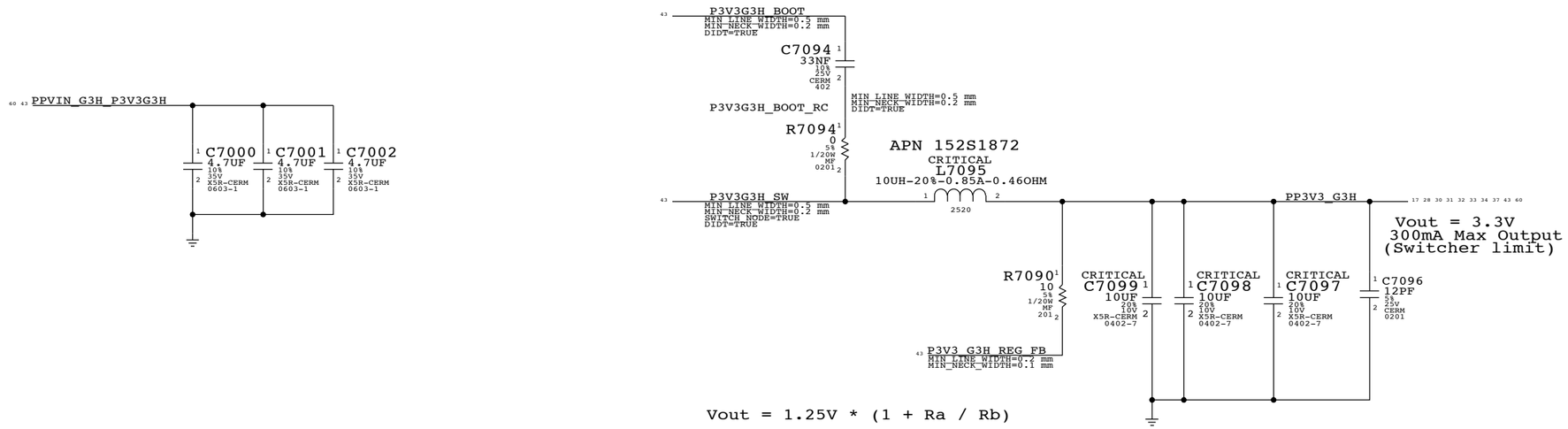
3.3V G3H VR - Bansuri



SYNC MASTER=J92 WILL SYNC DATE=02/04/2013

PAGE TITLE
3.3V G3Hot Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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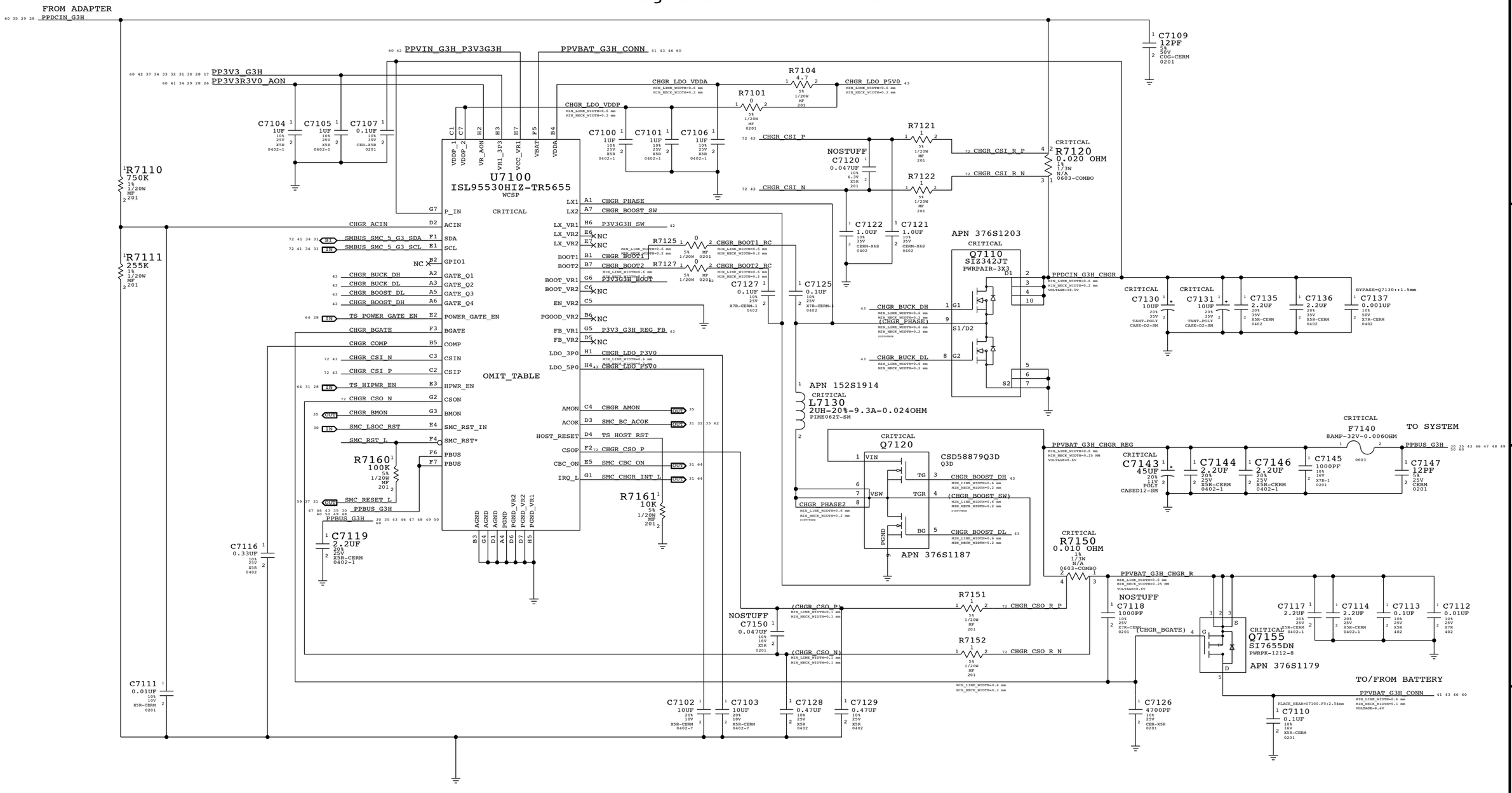
Charger PMIC - Bansuri



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00347	1	IC,ISL95530B1T11,CHGR PMU,BANSURI,WCSP56	U7100	CRITICAL	

SYNC MASTER=J92 DEVMLB SYNC DATE=04/04/2014

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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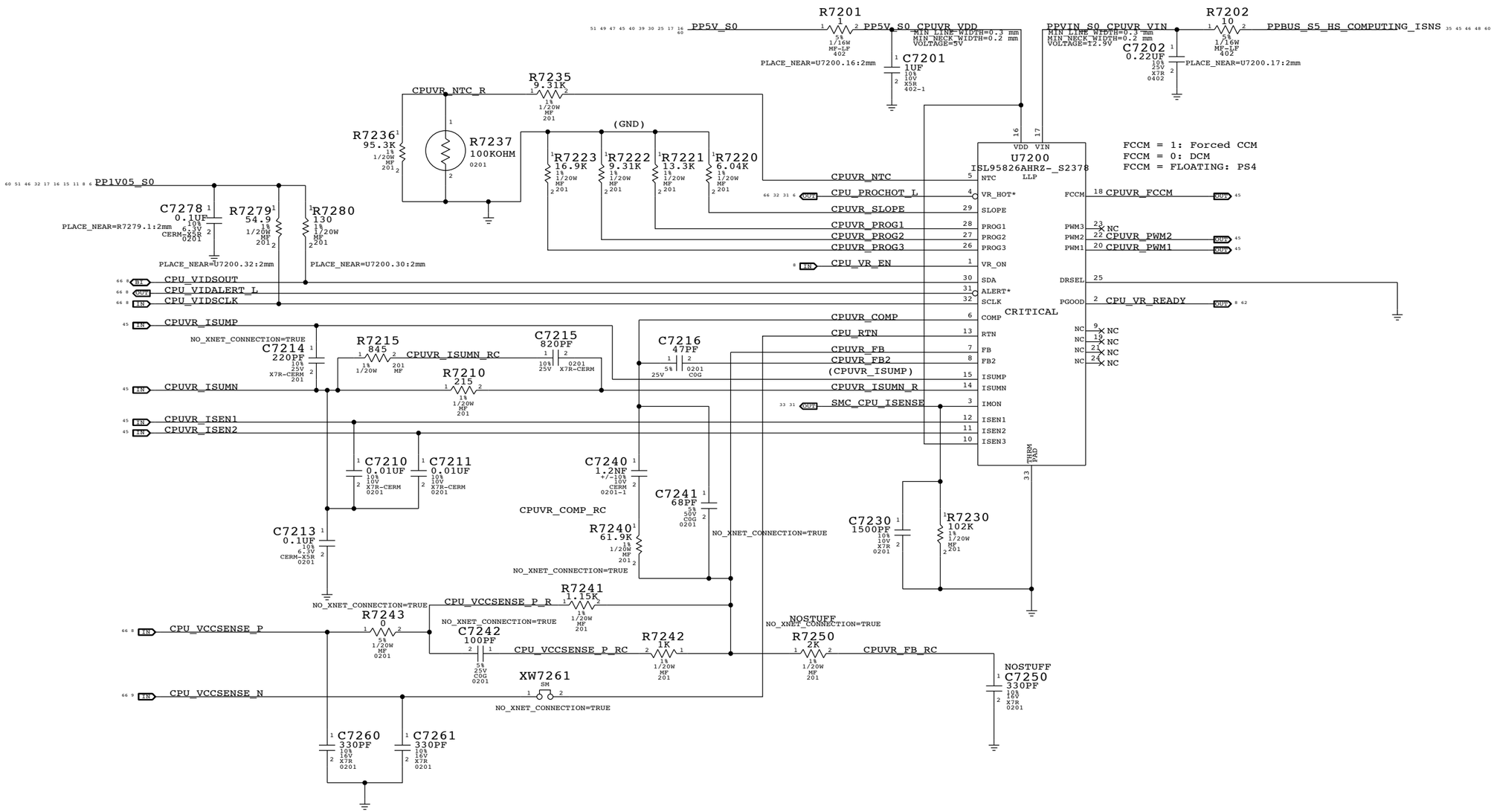

SYNC MASTER=J43 MLB SYNC DATE=10/09/2012

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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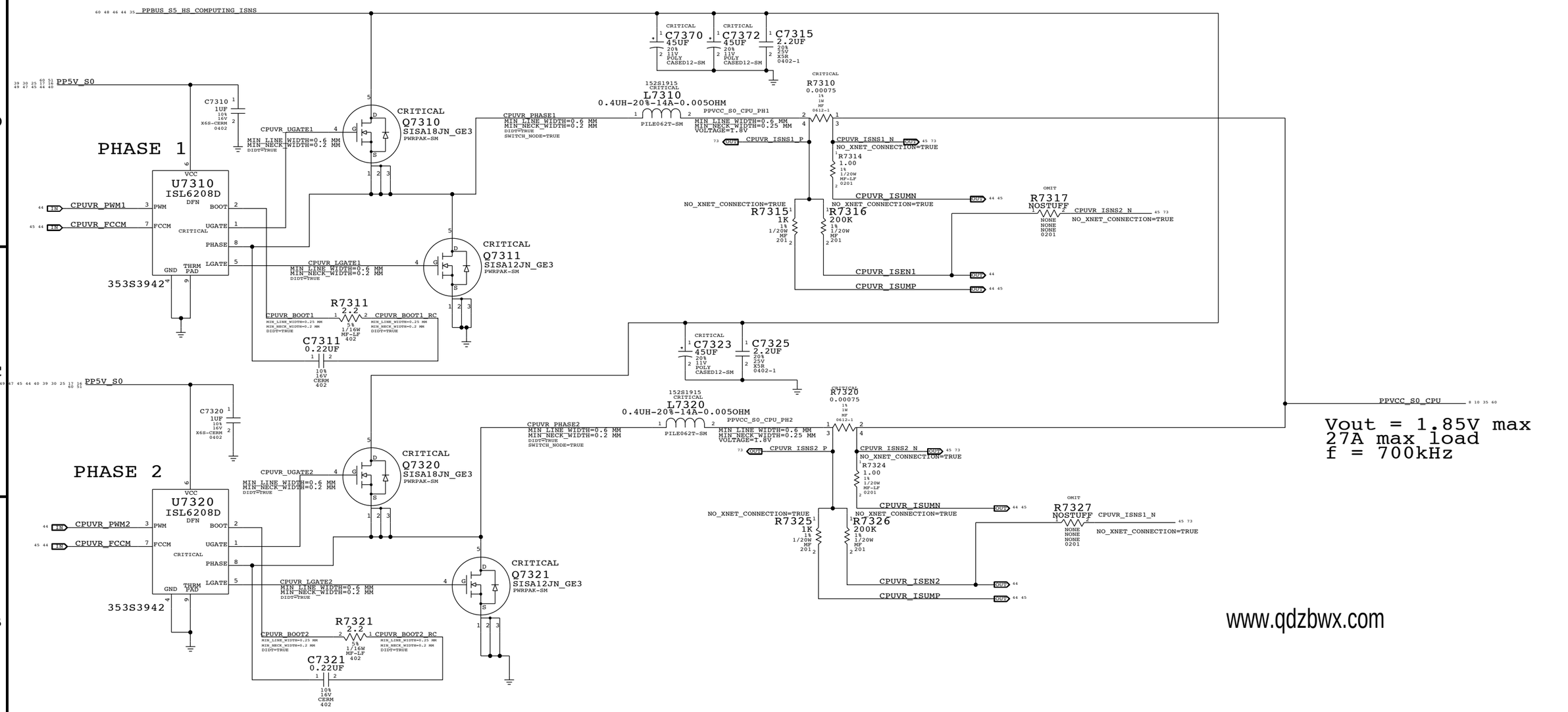

www.qdzbwx.com

SYNC MASTER=DEV_MLB	SYNC DATE=04/17/2014
PAGE TITLE: CPU VR12.5 VCC Power Stage	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 73 OF 130
	SHEET: 45 OF 75

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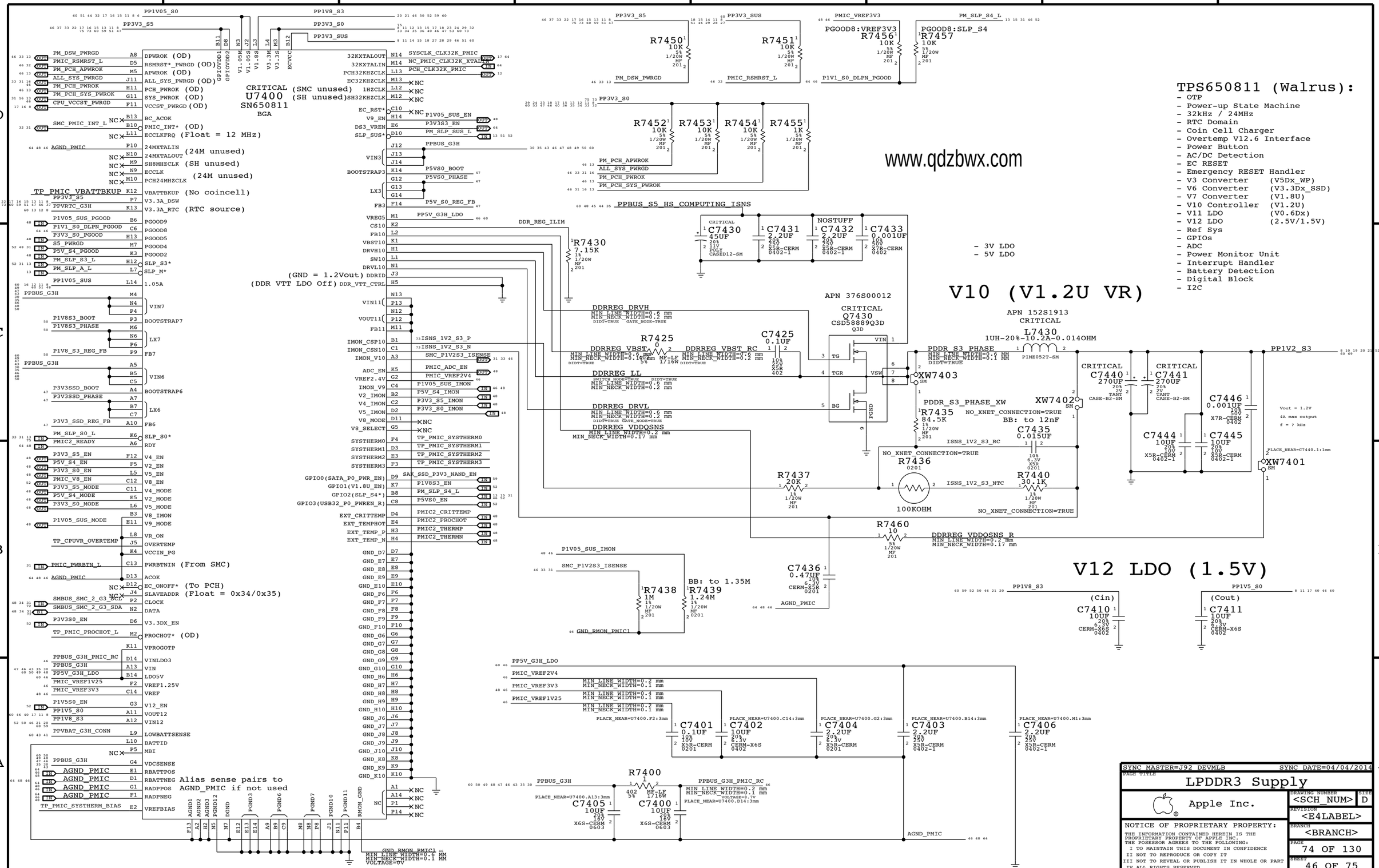

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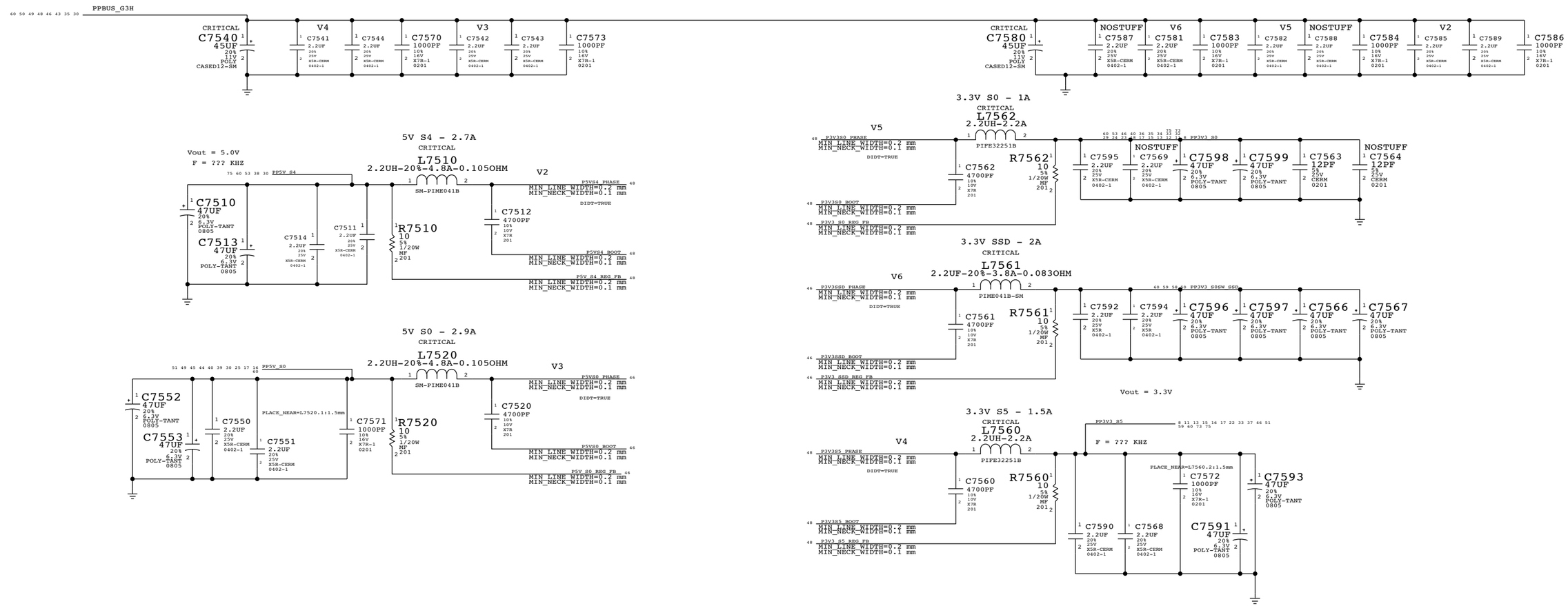

SYNC MASTER=DEV MLB SYNC DATE=04/17/2014

PAGE TITLE

5V & 3.3V Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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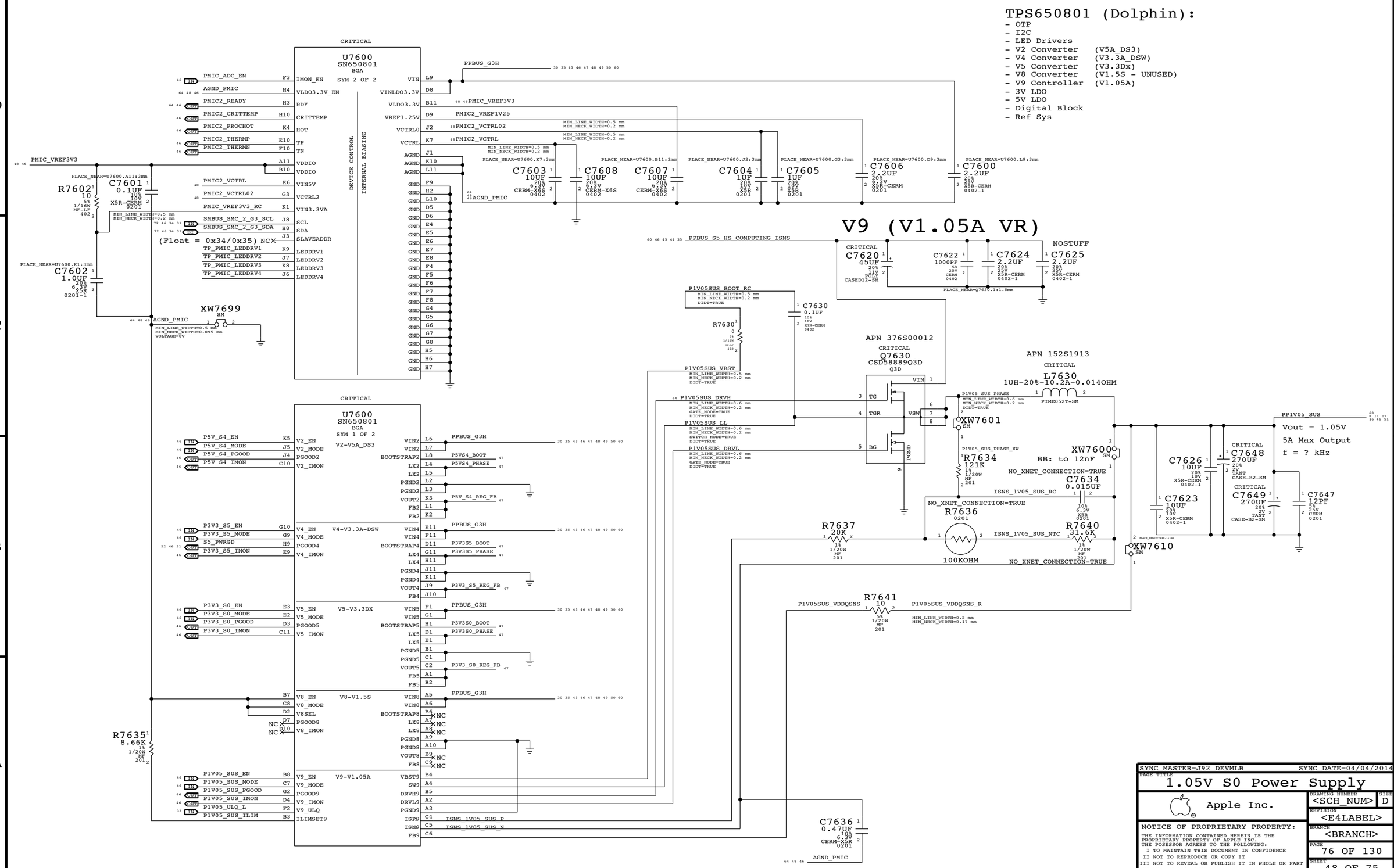
TPS650801 (Dolphin):
- OTP
- I2C
- LED Drivers
- V2 Converter (V5A_DS3)
- V4 Converter (V3.3A_DSW)
- V5 Converter (V3.3Dx)
- V8 Converter (V1.5S - UNUSED)
- V9 Controller (V1.05A)
- 3V LDO
- 5V LDO
- Digital Block
- Ref Sys
U7600
SN650801
BGA
SYM 2 OF 2
DEVICE CONTROL
INTERNAL BIASING
V9 (V1.05A VR)
APN 376S00012
Q7630
CSD58889Q3D
APN 152S1913
L7630
1UH-20%-10.2A-0.014OHM
XW7600
BB: to 12nF
XW7601
XW7610
XW7699
R7635
8.66K
Vout = 1.05V
5A Max Output
f = ? kHz
SYNC MASTER=J92 DEVMLB
SYNC DATE=04/04/2014
PAGE TITLE
1.05V S0 Power Supply
Apple Inc.
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<SCH_NUM>
SIZE
D
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<E4LABEL>
BRANCH
<BRANCH>
PAGE
76 OF 130
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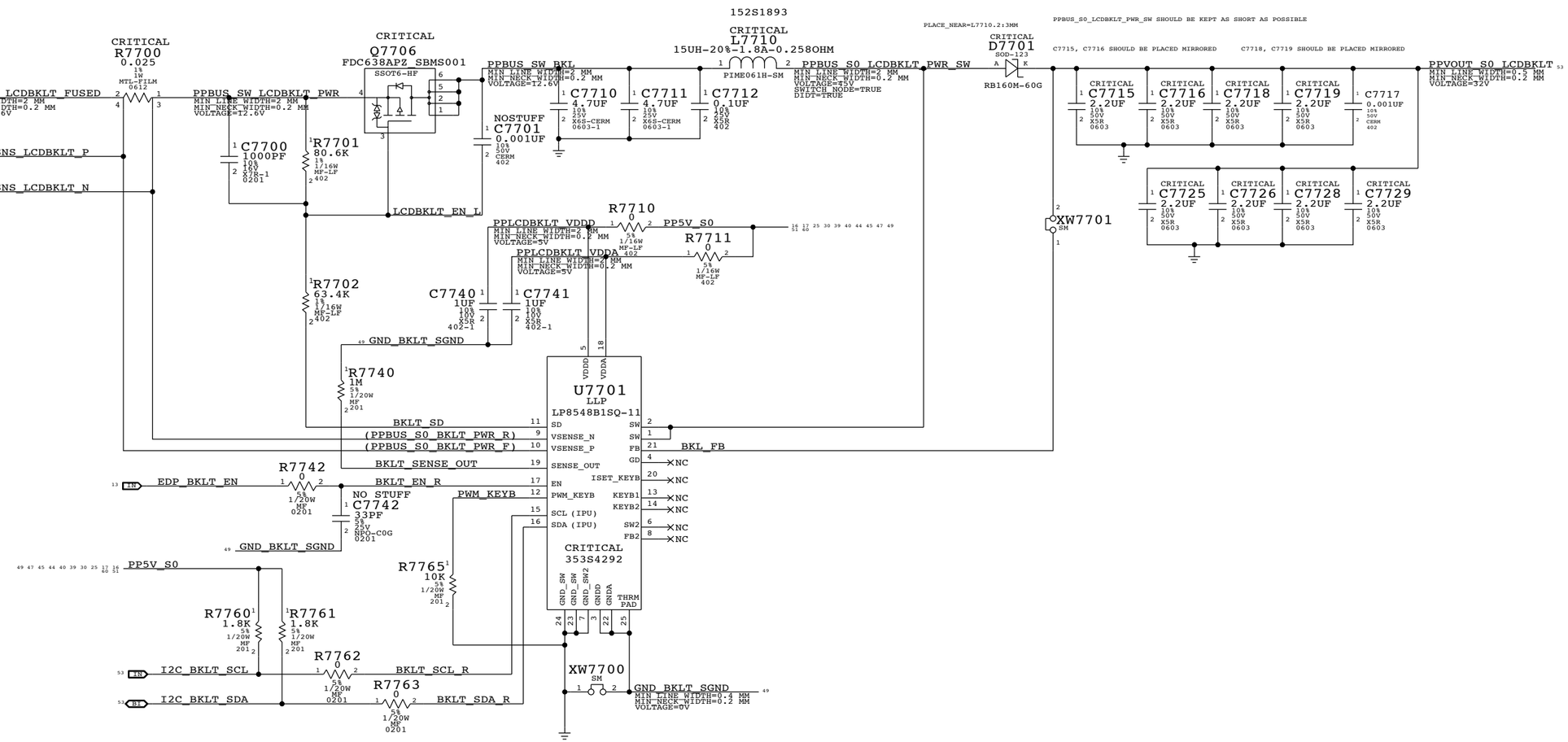
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (6-8.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production



SYNC MASTER=J92 DEVMLB SYNC DATE=10/01/2013

PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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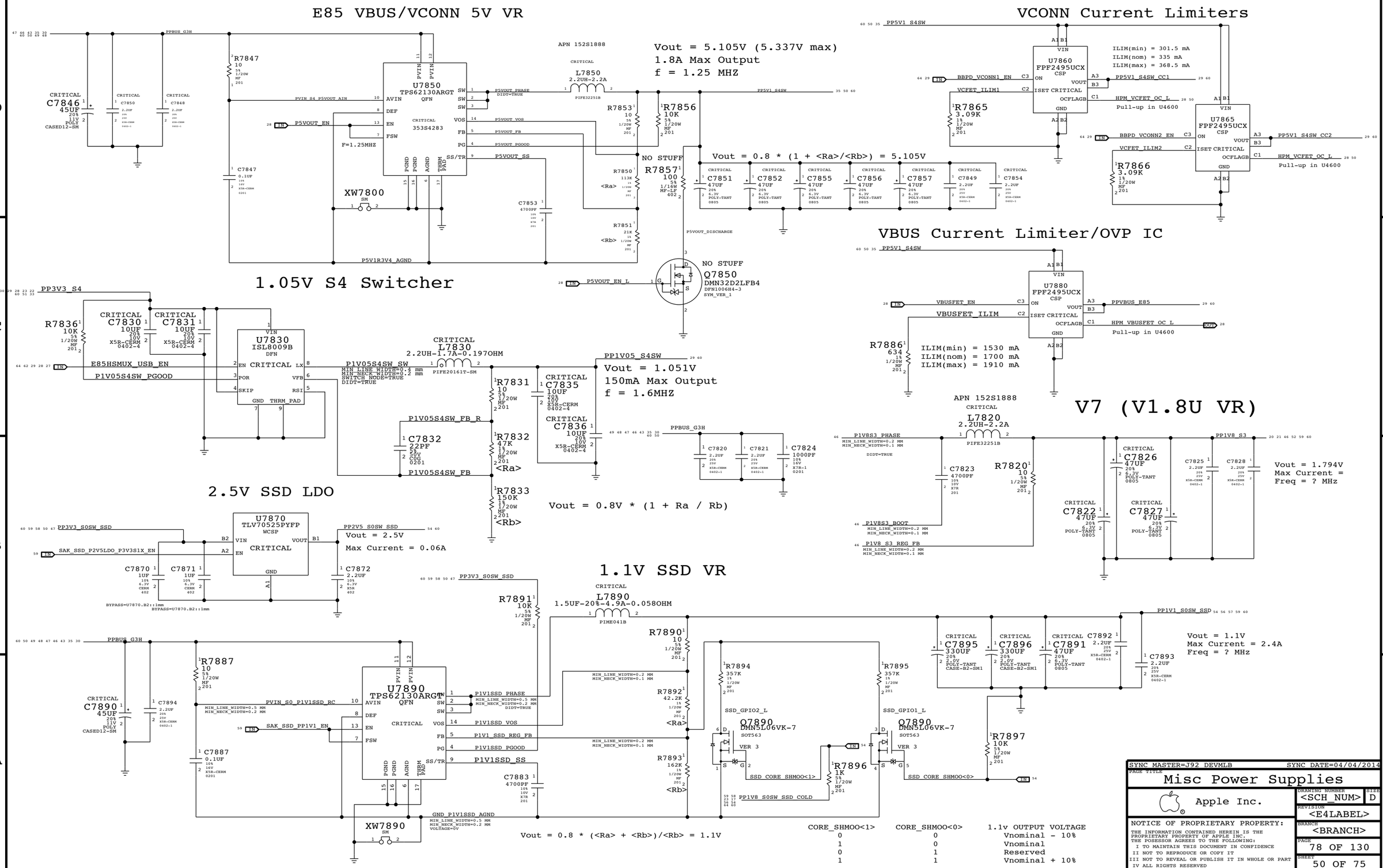
E85 VBUS/VCONN 5V VR
Vout = 5.105V (5.337V max)
1.8A Max Output
f = 1.25 MHZ
APN 152S1888
U7850
TPS62130ARGT
QFN
353S4283
F=1.25MHZ
Vout = 0.8 * (1 + <Ra>/<Rb>) = 5.105V
NO STUFF
Q7850
DMN32D2LFB4
1.05V S4 Switcher
VCONN Current Limiters
U7860
FPP2495UCX
CSP
U7865
ILIM(min) = 301.5 mA
ILIM(nom) = 335 mA
ILIM(max) = 368.5 mA
Pull-up in U4600
VBUS Current Limiter/OVP IC
U7880
ILIM(min) = 1530 mA
ILIM(nom) = 1700 mA
ILIM(max) = 1910 mA
U7830
ISL8009B
DFN
L7830
2.2UH-1.7A-0.197OHM
Vout = 1.051V
150mA Max Output
f = 1.6MHZ
Vout = 0.8V * (1 + Ra / Rb)
V7 (V1.8U VR)
L7820
2.2UH-2.2A
Vout = 1.794V
Max Current =
Freq = ? MHz
2.5V SSD LDO
U7870
TLV70525PYFP
WCSP
Vout = 2.5V
Max Current = 0.06A
1.1V SSD VR
L7890
1.5UF-20%-4.9A-0.058OHM
U7890
TPS62130ARGT
QFN
Vout = 1.1V
Max Current = 2.4A
Freq = ? MHz
Vout = 0.8 * (<Ra> + <Rb>)/<Rb> = 1.1V
CORE_SHMOO<1> CORE_SHMOO<0> 1.1v OUTPUT VOLTAGE
0 0 Vnominal - 10%
1 0 Vnominal
0 1 Reserved
1 1 Vnominal + 10%
SYNC MASTER=J92 DEVMLB SYNC DATE=04/04/2014
PAGE TITLE
Misc Power Supplies
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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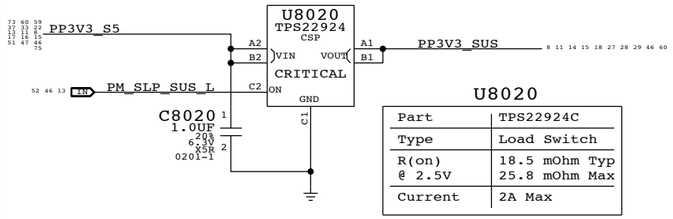
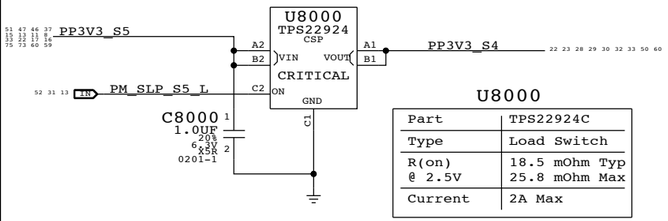
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

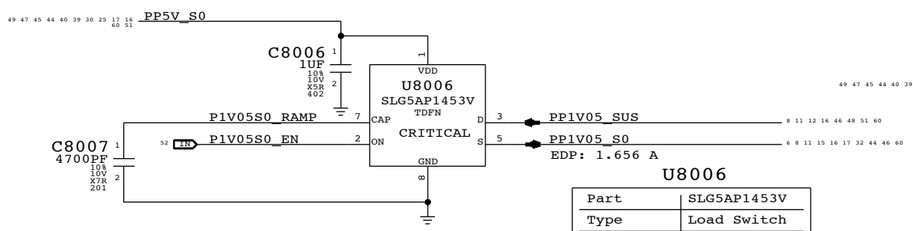
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

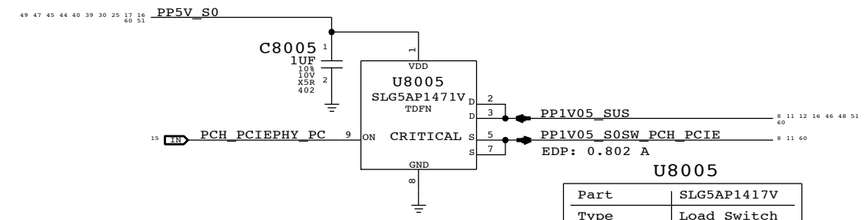
1.05V S0 Switch



U8006

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH PCIe Switch

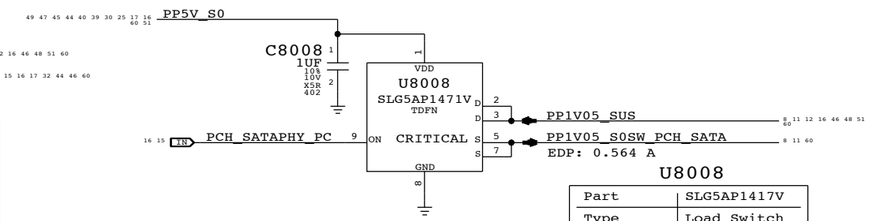


U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

1.05V PCH SATA Switch

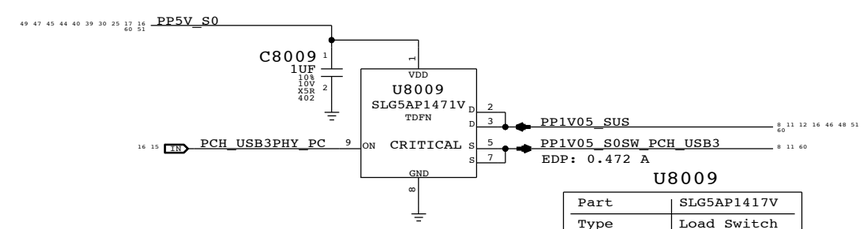


U8008

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

1.05V PCH USB3 Switch



U8009

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

SYNC MASTER=J92 DEVMLB SYNC DATE=07/24/2013

PAGE TITLE
Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SUS & S4 Enables

52 51 31 13 IN PM_SLP_S5_L MAKE_BASE=TRUE = PM_SLP_S5_L OUT 13 31 51 52

52 51 46 13 IN PM_SLP_SUS_L MAKE_BASE=TRUE = PM_SLP_SUS_L OUT 13 46 51 52

S3 Enables

46 IN PMIC_V8_EN — R8117 0 5% 1/20W MF 0201 — 2

46 31 15 13 IN PM_SLP_S4_L

NO STUFF D8115 0201 RB521ES-30 (A, K)

P1V8S3_EN_D

NO STUFF R8115 1K 5% 1/20W MF 201

NO STUFF R8116 30K 5% 1/20W MF 201

52 46 P1V8S3_EN MAKE_BASE=TRUE = P1V8S3_EN OUT 46 52

NO STUFF C8116 0.1UF 10% 6.3V CERM-X5R 0201

S5 Power Good

52 48 46 31 IN S5_PWRGD = S5_PWRGD MAKE_BASE=TRUE OUT 31 46 48 52

S0 Enables

46 31 13 IN PM_SLP_S3_L

D8182 0201 RB521ES-30 (K, A) — P1V5S0_EN_D — R8182 4.99K 1% 1/20W MF 201 — R8185 30K 5% 1/20W MF 201

D8181 0201 RB521ES-30 (K, A) — P3V3S0_EN_D — R8181 2.0K 5% 1/20W MF 201 — R8186 20K 5% 1/20W MF 201

D8183 0201 RB521ES-30 (A, K) — P1V05S0_EN_D — R8183 1K 5% 1/20W MF 201 — R8184 10K 5% 1/20W MF 201 — R8187 0 5% 1/20W MF 0201

C8185 0.1UF 10% 6.3V CERM-X5R 0201

C8186 0.1UF 10% 6.3V CERM-X5R 0201

C8184 0.1UF 10% 6.3V CERM-X5R 0201

NO STUFF C8187 0.1UF 10% 6.3V CERM-X5R 0201

52 46 P5VS0_EN MAKE_BASE=TRUE = P5VS0_EN OUT 46 52

52 51 P1V05S0_EN MAKE_BASE=TRUE = P1V05S0_EN OUT 51 52

52 46 P3V3S0_EN MAKE_BASE=TRUE = P3V3S0_EN OUT 46 52

52 46 P1V5S0_EN MAKE_BASE=TRUE = P1V5S0_EN OUT 46 52

LPDDR power down sequencing support

NO STUFF D8170 SOD-962 PMEG1201AESF (K, A)

PP1V8_S3 — 20 21 46 50 59 60

PP1V2_S3 — 8 10 19 20 21 46 59 60 69

SYNC MASTER=J92 DEVMLB SYNC DATE=09/20/2013

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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SHEET: 52 OF 75

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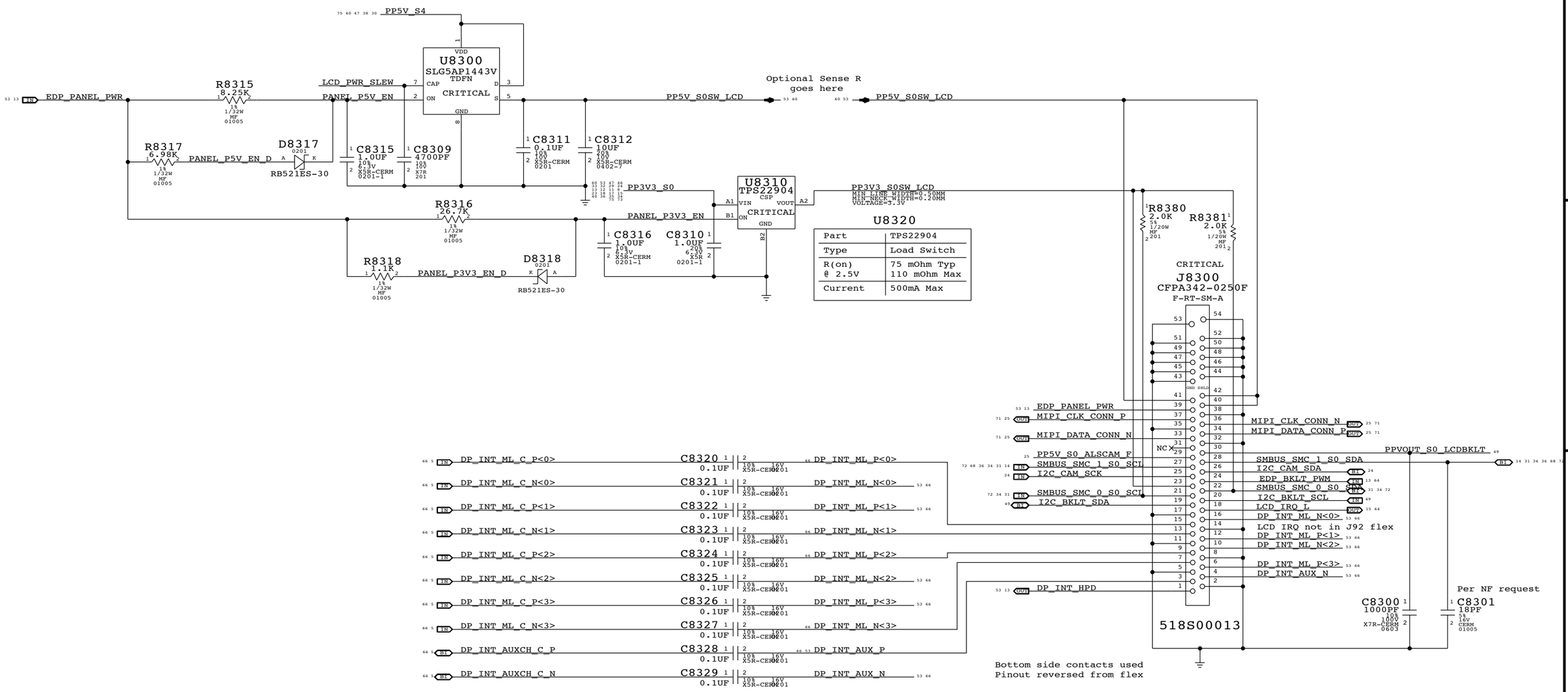
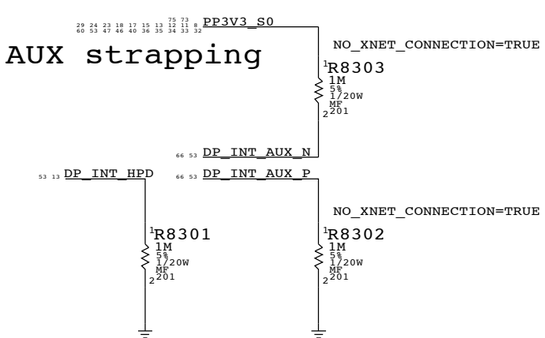
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



U8320

Part	TPS22904
Type	Load Switch
R(on) @ 2.5V	75 mOhm Typ 110 mOhm Max
Current	500mA Max

LCD Panel HPD & AUX strapping



SYNC MASTER=J92 DEVMLB SYNC DATE=09/25/2013

PAGE TITLE
eDP Display Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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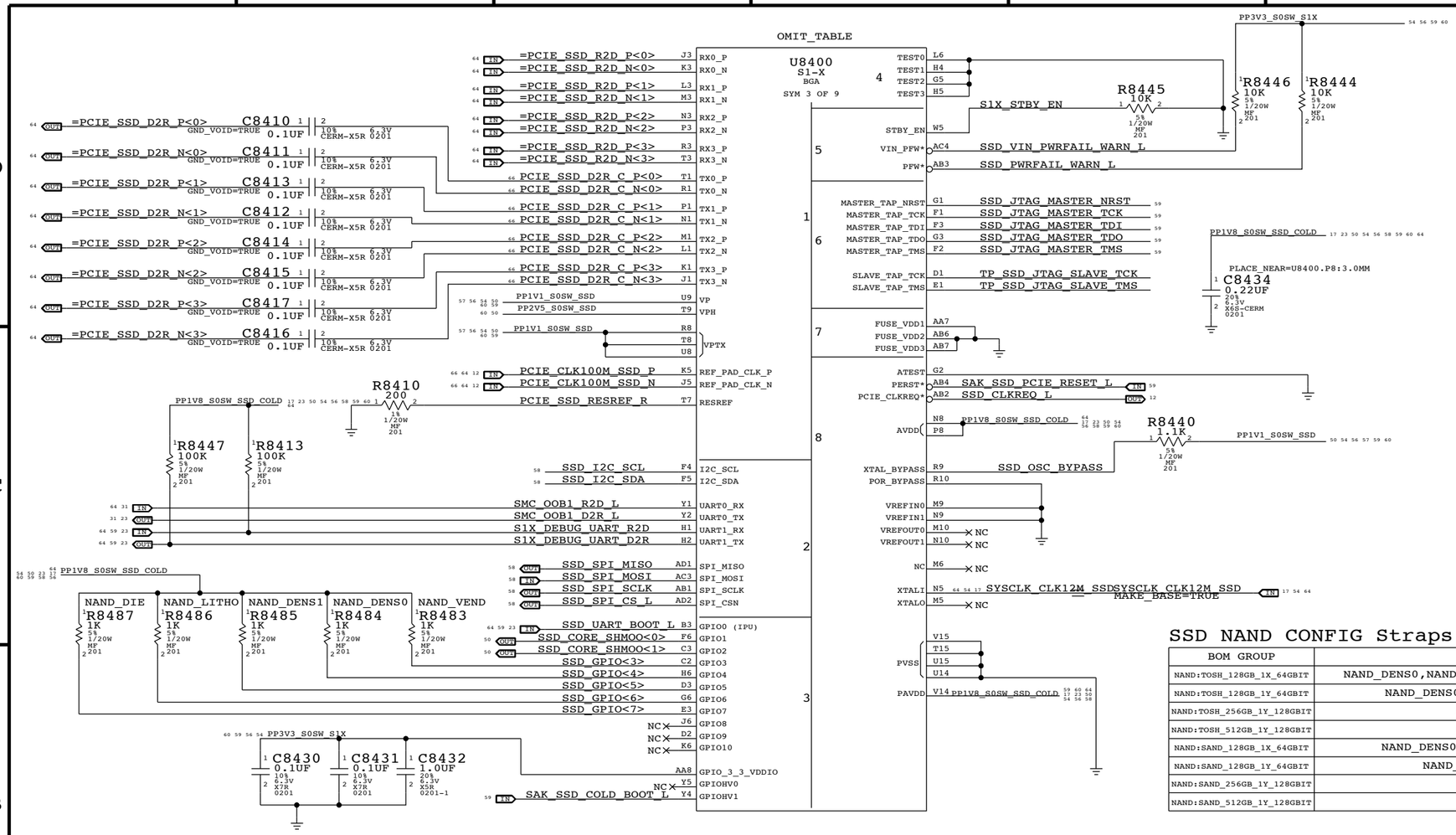

SSD NAND CONFIG Straps

BOM GROUP	BOM OPTIONS
NAND:TOSH_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_LITHO,NAND_DIE,NAND_TYPE:TOSH_128GB_1X_64GBIT
NAND:TOSH_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_DIE,NAND_TYPE:TOSH_128GB_1Y_64GBIT
NAND:TOSH_256GB_1Y_128GBIT	NAND_VEND,NAND_DENS1,NAND_TYPE:TOSH_256GB_1Y_128GBIT
NAND:TOSH_512GB_1Y_128GBIT	NAND_VEND,NAND_DENS0,NAND_TYPE:TOSH_512GB_1Y_128GBIT
NAND:SAND_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_LITHO,NAND_DIE,NAND_TYPE:SAND_128GB_1X_64GBIT
NAND:SAND_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_DIE,NAND_TYPE:SAND_128GB_1Y_64GBIT
NAND:SAND_256GB_1Y_128GBIT	NAND_DENS1,NAND_TYPE:SAND_256GB_1Y_128GBIT
NAND:SAND_512GB_1Y_128GBIT	NAND_DENS0,NAND_TYPE:SAND_512GB_1Y_128GBIT

SSD NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-7360	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1X_64GBIT
335S00004	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1Y_64GBIT
335S1031	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_256GB_1Y_128GBIT
335S1032	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_512GB_1Y_128GBIT
998-7361	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1X_64GBIT
335S1044	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1Y_64GBIT
335S1041	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_256GB_1Y_128GBIT
335S1045	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_512GB_1Y_128GBIT

S1-X GPIO[10:1] IPD

VENDOR	NAND_VEND(GPIO3)
TOSHIBA	1
SANDISK	0

DENSITY	NAND_DENS0(GPIO4)	NAND_DENS1(GPIO5)
128GB	1	1
256GB	0	1
512GB	1	0

LITHO	NAND_LITHO(GPIO6)
1X	1
1Y	0

DIE SIZE	NAND_DIE(GPIO7)
64Gb	1
128Gb	0

# NAND_CH	(GPIO8)
8 (X56)	1
4 (J92)	0

SYNC MASTER=J92 SSD SYNC DATE=02/11/2014

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SSD Controller (1 of 4)

Apple Inc.

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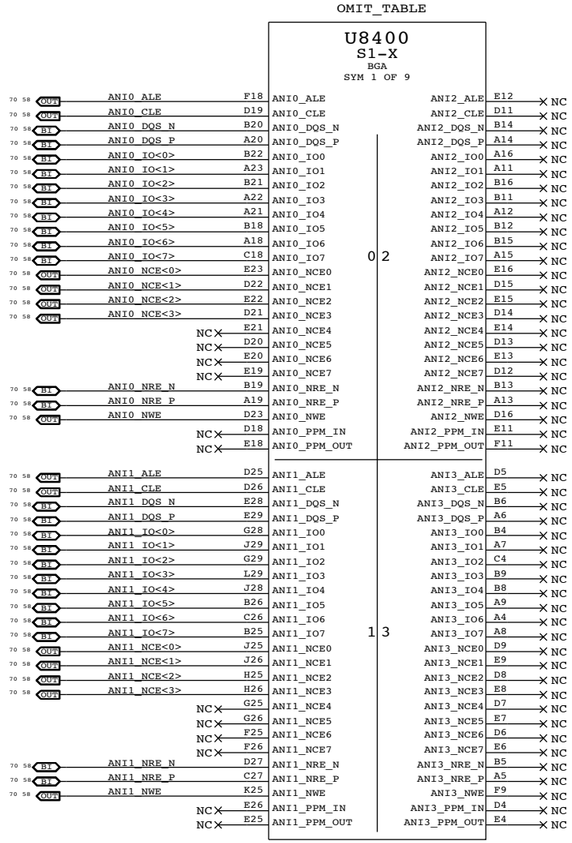

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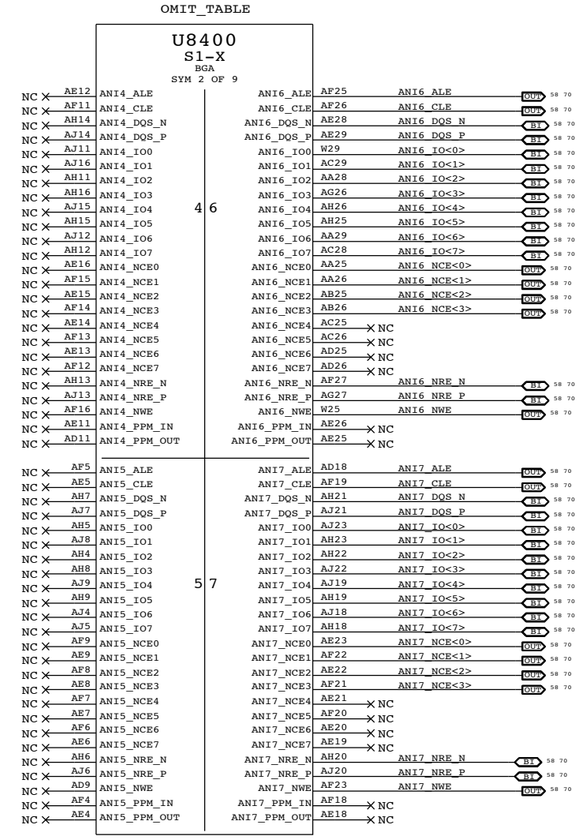

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PAGE TITLE: SSD Controller (2 of 4)	
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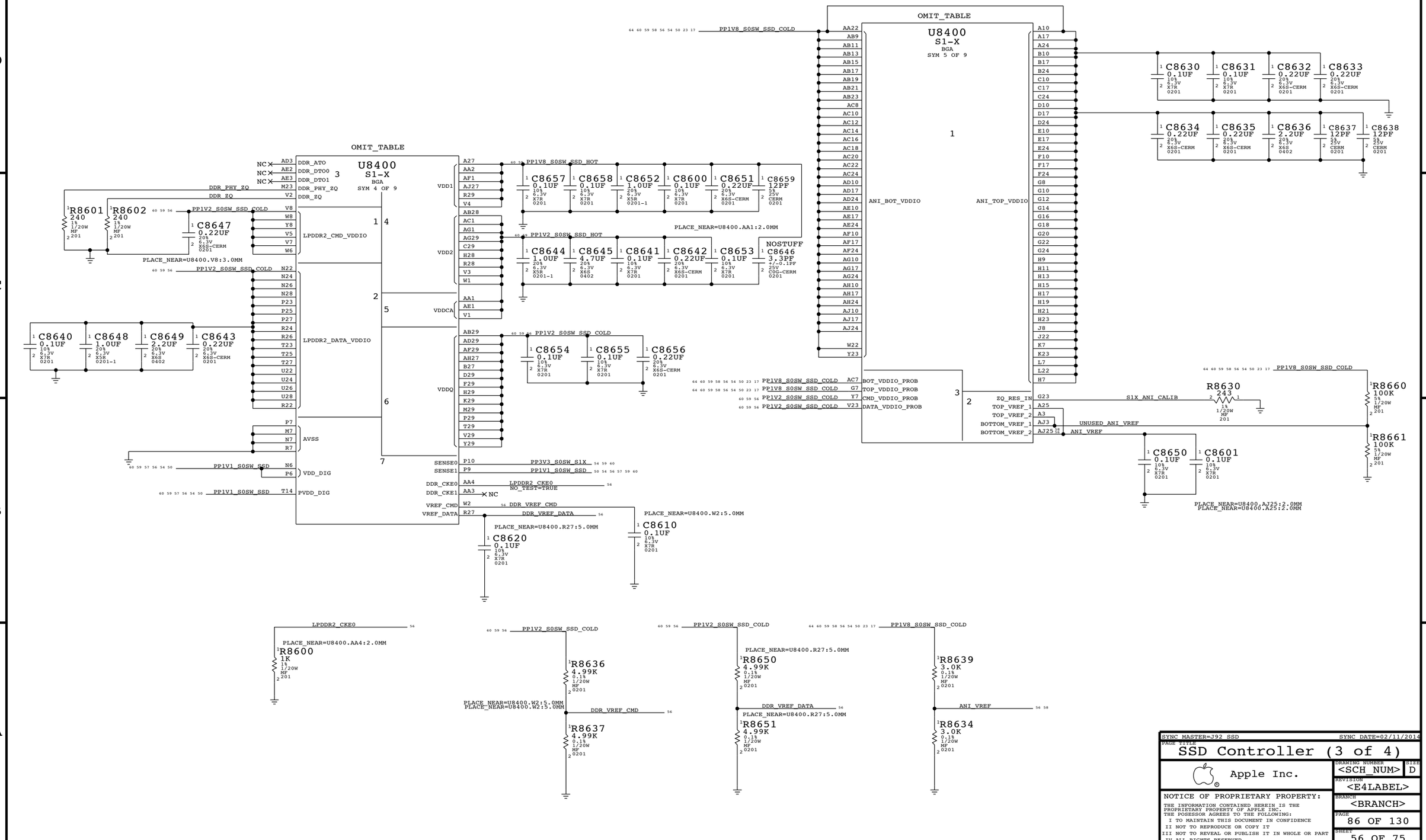

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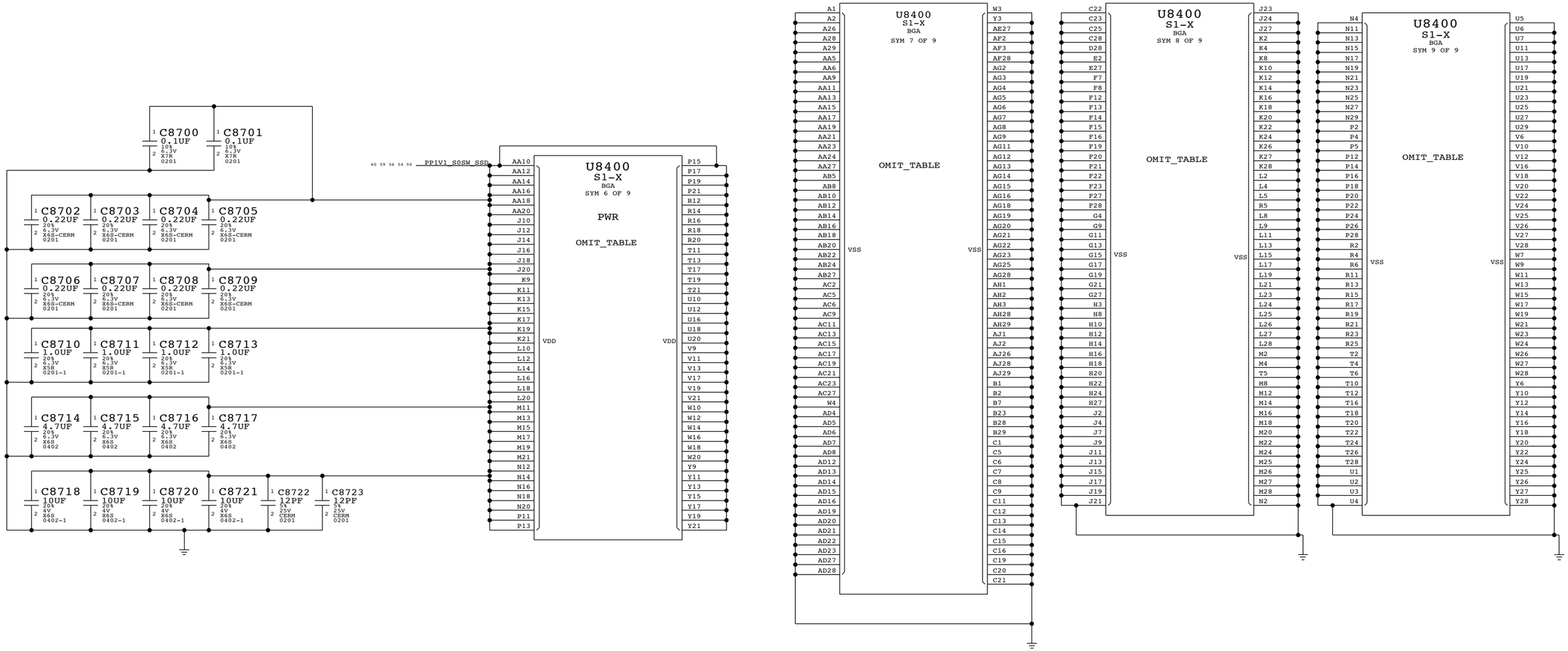

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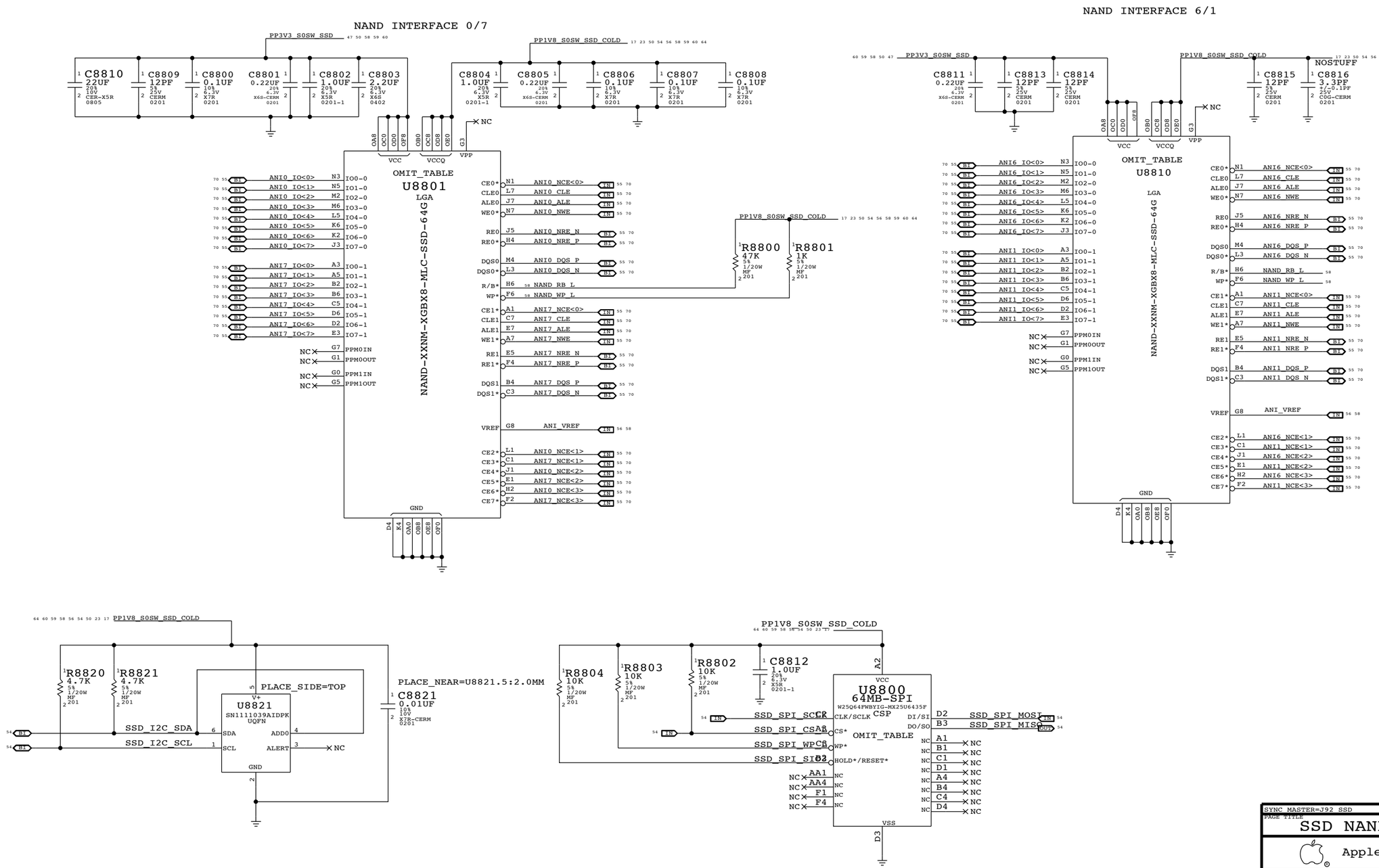

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PAGE TITLE

SSD NAND Flash & ROM

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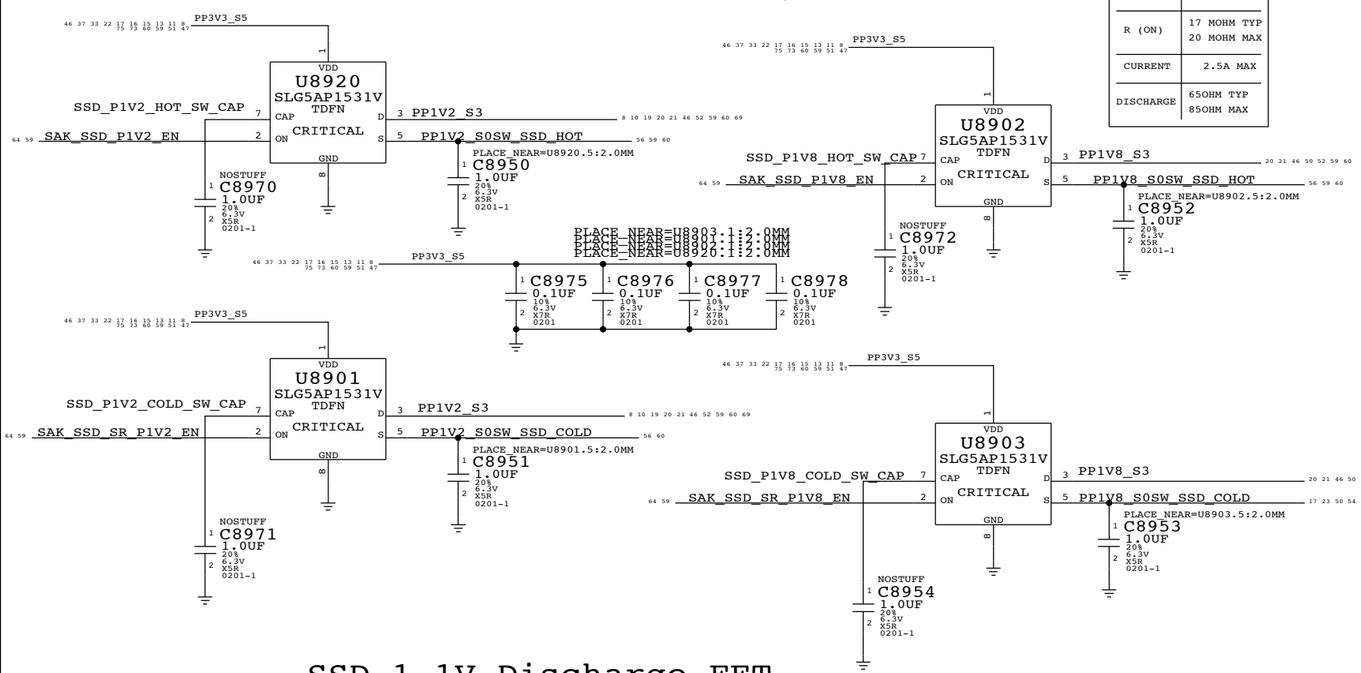
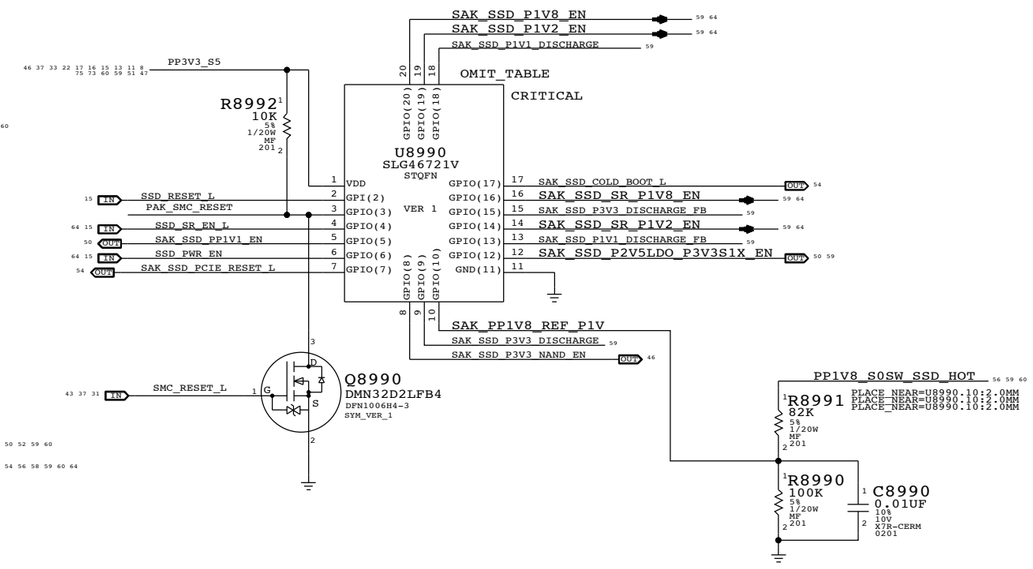
LPDDR2 1.2V & 1.8V LOAD SWITCHES FOR SEQUENCING, SR SUPPORT

PART	SLG5AP1531V
R (ON)	17 MOHM TYP 20 MOHM MAX
CURRENT	2.5A MAX
DISCHARGE	65OHM TYP 85OHM MAX

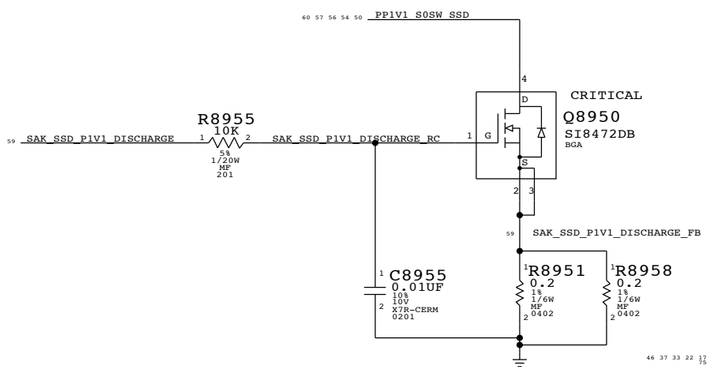


SILEGO GREEN PAK3 FOR POWER SEQUENCING, SR

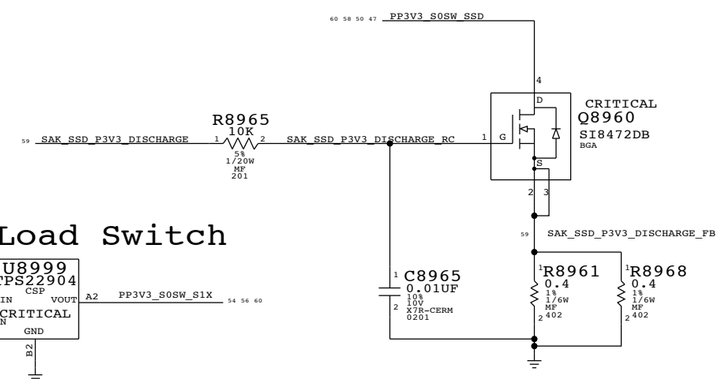


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00030	1	IC,SLG4AP4547V,PWR RAIL SEQUENCER,STQFN-20	U8990	CRITICAL	

SSD 1.1V Discharge FET

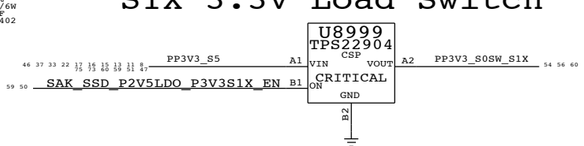


SSD 3.3V Discharge FET

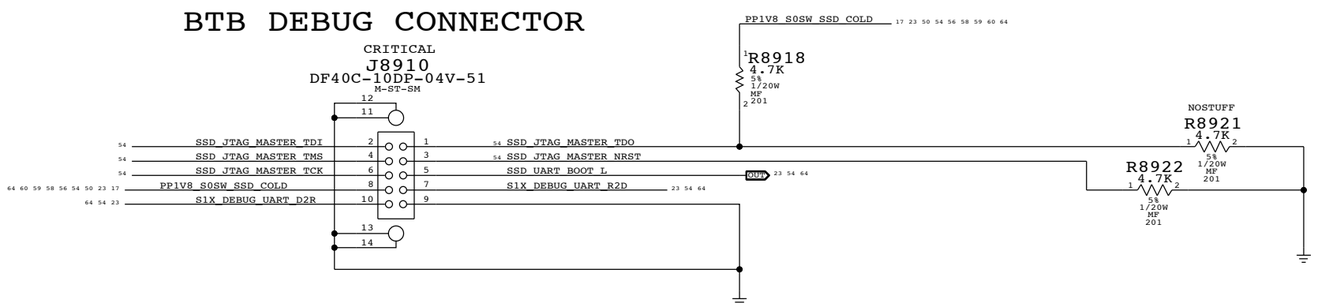


SSD 1.2V/1.8V HOT protection diode

S1X 3.3V Load Switch



BTB DEBUG CONNECTOR



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"G3Hot" (Always-Present) Rails

PPBUS_G3H
- PPBUS_G3H — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=8.6V, MAKE_BASE=TRUE
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H

PPVIN_G3H_P3V3G3H — PPVIN_G3H_P3V3G3H — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.6V, MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS — PPBUS_S5_HS_COMPUTING_ISNS — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.6V, MAKE_BASE=TRUE
- PPBUS_S5_HS_COMPUTING_ISNS
- PPBUS_S5_HS_COMPUTING_ISNS
- PPBUS_S5_HS_COMPUTING_ISNS

PPVBUS_E85 — PPVBUS_E85 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=20V, MAKE_BASE=TRUE
- PPVBUS_E85

PPDCIN_G3H — PPDCIN_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=20V, MAKE_BASE=TRUE
- PPDCIN_G3H
- PPDCIN_G3H
- PPDCIN_G3H

PP3V3_G3H — PP3V3_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H

PP3V3R3V0_AON — PP3V3R3V0_AON — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON

PPVRTC_G3H — PPVRTC_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3V, MAKE_BASE=TRUE
- PPVRTC_G3H

5V Rails

PP5V_G3H_LDO — PP5V_G3H_LDO — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.1 mm, VOLTAGE=5V, MAKE_BASE=TRUE

PP5V_S0SW_LCD — PP5V_S0SW_LCD — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V, MAKE_BASE=TRUE

PP5V_S4 — PP5V_S4 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S4
- PP5V_S4
- PP5V_S4

PP5V_S0 — PP5V_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.175 MM, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0

3.3V Rails

PP3V3_S5 — PP3V3_S5 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.15 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5

PP3V3_SUS — PP3V3_SUS — MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS

PP3V3_S4 — PP3V3_S4 — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4

PP3V3_S0 — PP3V3_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S0
- PP3V3_S0
- PP3V3_S0

Memory Bit/Byte Swizzle

LPDDR3 Command/Address

MAKE_BASE

	IN	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	OUT
	IN	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	OUT
	IN	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	OUT
	IN	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	OUT
	IN	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	OUT
	IN	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	OUT
69 61 20	IN	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	OUT
	IN	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	OUT
	IN	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	OUT
	IN	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	OUT
	IN	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	OUT
	IN	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	OUT
	IN	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	OUT
	IN	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	OUT
	IN	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	OUT
	IN	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	OUT
69 61 20	IN	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	OUT
	IN	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	OUT
	IN	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	OUT
	IN	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	OUT
69 61 20	IN	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	OUT
61	IN	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	
61	IN	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	
	IN	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	OUT
	IN	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>	OUT
	IN	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>	OUT
	IN	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>	OUT
	IN	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>	OUT
	IN	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>	OUT
69 61 21	IN	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	OUT
	IN	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	OUT
	IN	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>	OUT
	IN	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>	OUT
	IN	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	OUT
	IN	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>	OUT
	IN	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	OUT
	IN	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	OUT
	IN	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>	OUT
	IN	=MEM_B_A<2>	TRUE	MEM_B_CAB<5>	OUT
69 61 21	IN	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	OUT
	IN	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	OUT
	IN	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>	OUT
	IN	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>	OUT
69 61 21	IN	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	OUT
61	IN	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	
61	IN	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	

MAKE_BASE

	BI	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<34>	BI
	BI	=MEM_A_DQ<1>	TRUE	MEM_A_DQ<38>	BI
69 61 20	BI	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>	BI
	BI	=MEM_A_DQ<3>	TRUE	MEM_A_DQ<36>	BI
	BI	=MEM_A_DQ<4>	TRUE	MEM_A_DQ<35>	BI
	BI	=MEM_A_DQ<5>	TRUE	MEM_A_DQ<37>	BI
	BI	=MEM_A_DQ<6>	TRUE	MEM_A_DQ<32>	BI
	BI	=MEM_A_DQ<7>	TRUE	MEM_A_DQ<39>	BI
	BI	=MEM_A_DQ<8>	TRUE	MEM_A_DQ<44>	BI
	BI	=MEM_A_DQ<9>	TRUE	MEM_A_DQ<43>	BI
	BI	=MEM_A_DQ<10>	TRUE	MEM_A_DQ<46>	BI
	BI	=MEM_A_DQ<11>	TRUE	MEM_A_DQ<45>	BI
	BI	=MEM_A_DQ<12>	TRUE	MEM_A_DQ<42>	BI
	BI	=MEM_A_DQ<13>	TRUE	MEM_A_DQ<40>	BI
	BI	=MEM_A_DQ<14>	TRUE	MEM_A_DQ<47>	BI
	BI	=MEM_A_DQ<15>	TRUE	MEM_A_DQ<41>	BI
	BI	=MEM_A_DQ<16>	TRUE	MEM_A_DQ<55>	BI
	BI	=MEM_A_DQ<17>	TRUE	MEM_A_DQ<48>	BI
	BI	=MEM_A_DQ<18>	TRUE	MEM_A_DQ<54>	BI
	BI	=MEM_A_DQ<19>	TRUE	MEM_A_DQ<53>	BI
	BI	=MEM_A_DQ<20>	TRUE	MEM_A_DQ<49>	BI
	BI	=MEM_A_DQ<21>	TRUE	MEM_A_DQ<51>	BI
	BI	=MEM_A_DQ<22>	TRUE	MEM_A_DQ<50>	BI
	BI	=MEM_A_DQ<23>	TRUE	MEM_A_DQ<52>	BI
	BI	=MEM_A_DQ<24>	TRUE	MEM_A_DQ<61>	BI
	BI	=MEM_A_DQ<25>	TRUE	MEM_A_DQ<60>	BI
	BI	=MEM_A_DQ<26>	TRUE	MEM_A_DQ<63>	BI
	BI	=MEM_A_DQ<27>	TRUE	MEM_A_DQ<62>	BI
	BI	=MEM_A_DQ<28>	TRUE	MEM_A_DQ<57>	BI
	BI	=MEM_A_DQ<29>	TRUE	MEM_A_DQ<58>	BI
	BI	=MEM_A_DQ<30>	TRUE	MEM_A_DQ<56>	BI
	BI	=MEM_A_DQ<31>	TRUE	MEM_A_DQ<59>	BI
	BI	=MEM_A_DQ<32>	TRUE	MEM_A_DQ<2>	BI
	BI	=MEM_A_DQ<33>	TRUE	MEM_A_DQ<5>	BI
	BI	=MEM_A_DQ<34>	TRUE	MEM_A_DQ<7>	BI
	BI	=MEM_A_DQ<35>	TRUE	MEM_A_DQ<3>	BI
	BI	=MEM_A_DQ<36>	TRUE	MEM_A_DQ<6>	BI
	BI	=MEM_A_DQ<37>	TRUE	MEM_A_DQ<0>	BI
	BI	=MEM_A_DQ<38>	TRUE	MEM_A_DQ<1>	BI
	BI	=MEM_A_DQ<39>	TRUE	MEM_A_DQ<4>	BI
	BI	=MEM_A_DQ<40>	TRUE	MEM_A_DQ<14>	BI
	BI	=MEM_A_DQ<41>	TRUE	MEM_A_DQ<15>	BI
	BI	=MEM_A_DQ<42>	TRUE	MEM_A_DQ<8>	BI
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	BI	=MEM_A_DQ<44>	TRUE	MEM_A_DQ<10>	BI
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69 61 20	BI	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	BI
69 61 20	BI	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	BI
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MAKE_BASE

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61 21 69	BI	MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>	BI
	BI	=MEM_B_DQ<3>	TRUE	MEM_B_DQ<36>	BI
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61 21 69	BI	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	BI
61 21 69	BI	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	BI
	BI	=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<7>	BI
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	BI	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<2>	BI
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	BI	=MEM_B_DQS_N<7>	TRUE	MEM_B_DQS_N<3>	BI

61 6 TP_CPU_MEMVTT_PWR_EN_LSVDDO — TP_CPU_MEMVTT_PWR_EN_LSVDDO 6 61
MAKE_BASE=TRUE

SYNC MASTER=(MASTER) SYNC DATE=(MASTER)

PAGE TITLE
Memory Signal Swaps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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		MAKE_BASE		
64 62 28 15	OR_SWITCH_EN	TRUE	OR_SWITCH_EN	15 28 62 64
62 44 8	CPU_VR_READY	TRUE	CPU_VR_READY	8 44 62
62 31 13	SMC_PCH_SUSWARN_L	TRUE	SMC_PCH_SUSWARN_L	13 31 62
62 31 13	SMC_PCH_SUSACK_L	TRUE	SMC_PCH_SUSACK_L	13 31 62
62 43 35 32 31	SMC_BC_ACOK	TRUE	SMC_BC_ACOK	31 32 35 43 62
62 5	TP_ULX_SPARE1	TRUE	TP_ULX_SPARE1	5 62
62 5	TP_ULX_SSP_SPARE	TRUE	TP_ULX_SSP_SPARE	5 62
68 62 12	TP_LPC_CLK24M_LPCPLUS_R	TRUE	TP_LPC_CLK24M_LPCPLUS_R	12 62 68
64 62 28 13	HPM_I2C_INT_L	TRUE	HPM_I2C_INT_L	13 28 62 64
64 62 28 13	HPM_I2C_INT_L			
63 62 28 16 14 64	XDP_USB_EXTA_OC_L	TRUE	XDP_USB_EXTA_OC_L	14 16 28 62 63 64
62 37 32 31 26	SMC_TCK	TRUE	SMC_TCK	26 31 32 37 62
62 37 32 31 26	SMC_TMS	TRUE	SMC_TMS	26 31 32 37 62
62 28	TP_HPM_XTALOUT	TRUE	TP_HPM_XTALOUT	28 62
	GND	TRUE	GND	
68 64 62 29 12	PCIE_CLK100M_TBT_P	TRUE	PCIE_CLK100M_TBT_P	12 29 62 64 68
68 64 62 29 12	PCIE_CLK100M_TBT_N	TRUE	PCIE_CLK100M_TBT_N	12 29 62 64 68
29	=PCIE_E85_D2R_P	TRUE	PCIE_TBT_D2R_P<0>	14 68
29	=PCIE_E85_D2R_N	TRUE	PCIE_TBT_D2R_N<0>	14 68
29	=PCIE_E85_R2D_P	TRUE	PCIE_TBT_R2D_C_P<0>	14 68
29	=PCIE_E85_R2D_N	TRUE	PCIE_TBT_R2D_C_N<0>	14 68
62 29 12	TBT_CLKREQ_L	TRUE	TBT_CLKREQ_L	12 29 62
62 29 15	PCH_TBT_PCIE_RESET_L	TRUE	PCH_TBT_PCIE_RESET_L	15 29 62
64 62 29 28	E85_TEST_MODE_L	TRUE	E85_TEST_MODE_L	28 29 62 64

64 62 50 29 28 27 IN E85HSMUX_USB_EN — E85HSMUX_USB_EN OUT 27 28 29 50 62 64
MAKE_BASE=TRUE

SYNC MASTER=J92 DEVMLB SYNC DATE=07/08/2014

PAGE TITLE
J92 Signal Aliases

Apple Inc.

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NO_TEST Nets

		NO_TEST	MAKE_BASE			
63 12	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	12 63	CPU/PCH
63 12	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	12 63	
63	NC_PCIE_TBT_D2RP<1>	TRUE	TRUE	NC_PCIE_TBT_D2RP<1>	63	
63	NC_PCIE_TBT_D2RN<1>	TRUE	TRUE	NC_PCIE_TBT_D2RN<1>	63	
63	NC_PCIE_TBT_R2D_CP<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CP<1>	63	
63	NC_PCIE_TBT_R2D_CN<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CN<1>	63	
63 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 63	
63 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 63	
63 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 63	
63 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 63	
63 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 63	
63 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 63	
63 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 63	
63 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 63	
63 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 63	
	=DP_TBTSNK1_ML_C_P<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CP<3..0>	5	
	=DP_TBTSNK1_ML_C_N<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CN<3..0>	5	
63 13	NC_DP_TBTSNK1_DDC_CLK	TRUE	TRUE	NC_DP_TBTSNK1_DDC_CLK	13 63	
63 13	NC_DP_TBTSNK1_DDC_DATA	TRUE	TRUE	NC_DP_TBTSNK1_DDC_DATA	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CP	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CN	13 63	
63 13	NC_DP_TBTSNK1_HPD	TRUE	TRUE	NC_DP_TBTSNK1_HPD	13 63	
63 31	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	31 63	SMC
63	NC_SMC_DEBUGPRT_EN_L	TRUE	TRUE	NC_SMC_DEBUGPRT_EN_L	63	
63 31	NC_SMC_SYS_KBDLED	TRUE	TRUE	NC_SMC_SYS_KBDLED	31 63	
63	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	63	
63 31	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	31 63	
63 31	NC_SMC_FAN_0_TACH	TRUE	TRUE	NC_SMC_FAN_0_TACH	31 63	
63 31	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	31 63	
63 31	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	31 63	
64 63 31	NC_SYS_ONEWIRE	TRUE	TRUE	NC_SYS_ONEWIRE	31 63 64	

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
SD_PWR_EN	15
ENET_MEDIA_SENSE	15
BT_PWRRST_L	15
TPAD_USB_IF_EN	15
PCH_GPIO12	15
TBT_PWR_EN	15
TBT_CIO_PLUG_EVENT_L	15
JTAG_TBT_TMS_PCH	15
ODD_PWR_EN_L	13
HDMITBTMUX_FLAG	13
HDMITBTMUX_LATCH	13
CAM_SENSOR_WAKE_L	24
LCD_PSR_EN	15
XDP_USB_EXTA_OC_L	14 16 28 62 64
AUD_WAKE_L	15
MIKEY_SPI_CS_L	15
MIKEY_SPI_CLK	15
MIKEY_SPI_MISO	15
MIKEY_SPI_MOSI	15

SYNC MASTER=J92 DEVMLB SYNC DATE=07/08/2014

PAGE TITLE

Func Test / No Test

Apple Inc.

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EE Chaz Probe Points

PPA501 P3V3S3_EN — P3V3S3_EN (MAKE_BASE=TRUE)
PPA502 PMIC2_READY
PPA503 P1V05SUS_DRVH
PPA504 SMC_CBC_ON
PPA505 SMC_CHGR_INT_L
PPA506 MEM_B_CAA<0>
PPA507 MEM_B_CLK_P<0>
PPA508 MEM_B_CLK_N<0>
PPA509 MEM_B_CS_L<0>
PPA510 MEM_B_DQ<0>
PPA511 MEM_B_DQS_P<0>
PPA512 MEM_B_DQS_N<0>
PPA513 AP_PCIE_DEV_WAKE
PPA514 AP_S0IX_WAKE_L
PPA515 AP_S0IX_WAKE_SEL
PPA516 E85HSMUX_USB_EN

PPA519 PCH_BT_UART_D2R
PPA520 BT_UART_CTS_L
PPA521 PCH_UART1_R2D
PPA522 PCIE_CAMERA_D2R_P
PPA523 PCIE_CLK100M_SSD_P
PPA524 PCIE_CLK100M_TBT_P

AGND_PMIC — AGND_PMIC (MAKE_BASE=TRUE)
AGND_PMIC
AGND_PMIC
AGND_PMIC
AGND_PMIC

TS_HIPWR_EN — TS_HIPWR_EN (MAKE_BASE=TRUE)
TS_POWER_GATE_EN — TS_POWER_GATE_EN (MAKE_BASE=TRUE)
SSD_PWR_EN — SSD_PWR_EN (MAKE_BASE=TRUE)
SSD_UART_BOOT_L — SSD_UART_BOOT_L (MAKE_BASE=TRUE)
S1X_DEBUG_UART_D2R — S1X_DEBUG_UART_D2R (MAKE_BASE=TRUE)
S1X_DEBUG_UART_R2D — S1X_DEBUG_UART_R2D (MAKE_BASE=TRUE)
PP1V8_S0SW_SSD_COLD — PP1V8_S0SW_SSD_COLD (MAKE_BASE=TRUE)
PCIE_CLK100M_SSD_P — PCIE_CLK100M_SSD_P (MAKE_BASE=TRUE)
PCIE_CLK100M_SSD_N — PCIE_CLK100M_SSD_N (MAKE_BASE=TRUE)
=PCIE_SSD_D2R_P<0..3> — PCIE_SSD_D2R_P<0..3> (MAKE_BASE=TRUE)
=PCIE_SSD_D2R_N<0..3> — PCIE_SSD_D2R_N<0..3> (MAKE_BASE=TRUE)
=PCIE_SSD_R2D_P<0..3> — PCIE_SSD_R2D_P<0..3> (MAKE_BASE=TRUE)
=PCIE_SSD_R2D_N<0..3> — PCIE_SSD_R2D_N<0..3> (MAKE_BASE=TRUE)
P1V1_S0_DLPN_PGOOD — P1V1_S0_DLPN_PGOOD (MAKE_BASE=TRUE)
SYSCLK_CLK24M_CAMERA — SYSCLK_CLK24M_CAMERA (MAKE_BASE=TRUE)
SYSCLK_CLK32K_PMIC — SYSCLK_CLK32K_PMIC (MAKE_BASE=TRUE)
TP_SMC_PWRFAIL_WARN_L — TP_SMC_PWRFAIL_WARN_L (MAKE_BASE=TRUE)

PPA525 E85_RFU<1>
PPA526 E85_RFU<2>
PPA527 E85_CC1
PPA528 E85_CC2
PPA529 AUD_PWR_EN
PPA530 BT_UART_RTS_L
PPA531 CAMERA_PWR_EN
PPA532 HPM_I2C_INT_L
PPA533 EDP_BKLT_PWM
PPA534 HDA_SDIN0
PPA535 I2C_PCH_1_SCL
PPA536 I2C_PCH_1_SDA
PPA537 LCD_IRQ_L
PPA538 MEM_CAM_A<8>
PPA539 MEM_CAM_CS_L

PPA545 PCH_BT_UART_CTS_L
PPA546 PCH_BT_UART_R2D
PPA547 PCH_UART1_D2R
PPA548 PCIE_CAMERA_D2R_N
PPA549 PCIE_CLK100M_SSD_N
PPA550 PCIE_CLK100M_TBT_N
PPA551 PCIE_SSD_D2R_N<0>
PPA552 PCIE_SSD_D2R_P<0>

PPA555 QR_SWITCH_EN
PPA556 SAK_SSD_P1V2_EN
PPA557 SAK_SSD_P1V8_EN
PPA558 SAK_SSD_SR_P1V2_EN
PPA559 SAK_SSD_SR_P1V8_EN
PPA560 SMC_BT_PWR_EN
PPA561 SMC_CLK32K_PMIC
PPA562 SMC_OOB1_R2D_L
PPA563 SMC_PROCHOT
PPA564 SMC_SENSOR_PWR_EN
PPA565 SMC_WAKE_SCI_L
PPA566 SMC_WIFI_PWR_EN
PPA567 AP_PCIE_WAKE_L
PPA568 SSD_BOOT
PPA569 SSD_SR_EN_L
PPA570 SYSCLK_CLK12M_SMC
PPA571 SYSCLK_CLK12M_SSD
PPA572 SYSCLK_CLK24M_CAMERA
PPA573 SYSCLK_CLK32K_PMIC
PPA574 BT_DEV_WAKE
PPA575 TPAD_SPI_CS_L
PPA576 TPAD_SPI_INT_L

PPA577 USB3_EXTA_D2R_N
PPA578 USB3_EXTA_D2R_P
PPA579 CPU_CATERR_L
PPA580 E85_TEST_MODE_L
PPA581 MEM_B_CS_L<1>
PPA582 MEM_B_CKE<1>
PPA583 MEM_B_CAB<1>
PPA584 MEM_B_CAA<2>
PPA585 MCP_RSVD_CK13 — MCP_RSVD_CK13 (MAKE_BASE=TRUE)
PPA586 MCP_DC_CV45 — MCP_DC_CV45 (MAKE_BASE=TRUE)
PPA587 MEM_B_CAA<3>
PPA588 E85_LS_P<1>
PPA589 E85_LS_N<1>
PPA590 E85_LS_P<2>
PPA591 E85_LS_N<2>
PPA592 XDP_PCH_UART_SSD_L_BT_H
PPA593 DP_E85SNK_HPD
PPA594 XDP_USB_EXTA_OC_L
PPA595 XDP_USB_EXTB_OC_L
PPA596 USB_EXTA_P
PPA597 USB_EXTA_N

PPA5A0 BBPD_IPU_EN
PPA5A1 BBPD_MISO_LS1V1
PPA5A2 BBPD_PD_EN
PPA5A3 BBPD_PD_SEL_CC2
PPA5A4 BBPD_RPD_EN
PPA5A5 BBPD_RX_L_TX_H
PPA5A6 BBPD_SPI_MOSI
PPA5A7 BBPD_VCONN1_EN
PPA5A8 BBPD_VCONN2_EN
PPA5A9 BBPD_VCONN_EN

TP_ULX_DDR_VCCDDQG — TP_ULX_DDR_VCCDDQG (TRUE)
SMC_DEBUGPRT_TX_L — SMC_DEBUGPRT_TX_L (TRUE)
SMC_DEBUGPRT_RX_L — SMC_DEBUGPRT_RX_L (TRUE)

NO_TEST Nets

NC_USB3_EXTB_D2RP — NC_USB3_EXTB_D2RP (TRUE TRUE)
NC_USB3_EXTB_D2RN — NC_USB3_EXTB_D2RN (TRUE TRUE)
NC_USB3_EXTB_R2D_CP — NC_USB3_EXTB_R2D_CP (TRUE TRUE)
NC_USB3_EXTB_R2D_CN — NC_USB3_EXTB_R2D_CN (TRUE TRUE)
NC_USB_IRP — NC_USB_IRP (TRUE TRUE)
NC_USB_IRN — NC_USB_IRN (TRUE TRUE)
NC_USB_EXTBP — NC_USB_EXTBP (TRUE TRUE)
NC_USB_EXTBN — NC_USB_EXTBN (TRUE TRUE)
NC_USB_TPADP — NC_USB_TPADP (TRUE TRUE)
NC_USB_TPADN — NC_USB_TPADN (TRUE TRUE)
NC_PCIE_CLK100M_FWP — NC_PCIE_CLK100M_FWP (TRUE TRUE)
NC_PCIE_CLK100M_FWN — NC_PCIE_CLK100M_FWN (TRUE TRUE)

CPU/PCH

NC_SYS_ONEWIRE — NC_SYS_ONEWIRE (TRUE TRUE)
NC_PMIC_CLK32K_XTALIN — NC_PMIC_CLK32K_XTALIN (TRUE TRUE)
NC_SMC_GFX_OVERTEMP — NC_SMC_GFX_OVERTEMP (TRUE TRUE)
NC_SMC_FAN_0_CTL — NC_SMC_FAN_0_CTL (TRUE TRUE)
NC_SMC_FAN_4_CTL — NC_SMC_FAN_4_CTL (TRUE TRUE)

Unused nets with offpage

(Nets with offpages not used on this project)

XDP_USB_EXTB_OC_L

SYNC MASTER=J41 MLB — SYNC DATE=10/24/2012

PAGE TITLE: Project FCT/NC/Aliases

Apple Inc.

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J92 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL6,ISL8,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL4	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	Y	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.260 MM			
27P4_OHM_SE	ISL6,ISL8,ISL10	Y	0.134 MM	0.134 MM			
27P4_OHM_SE	ISL3,ISL4	Y	0.190 MM	0.190 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.144 MM	0.144 MM			
40_OHM_SE	ISL6	Y	0.070 MM	0.070 MM			
40_OHM_SE	ISL8	Y	0.073 MM	0.073 MM			
40_OHM_SE	ISL10	Y	0.071 MM	0.071 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.095 MM			
45_OHM_SE	ISL6	Y	0.057 MM	0.057 MM			
45_OHM_SE	ISL8	Y	0.058 MM	0.058 MM			
45_OHM_SE	ISL10	Y	0.057 MM	0.057 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
50_OHM_SE_RF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.147 MM	0.060 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL6	Y	0.082 MM	0.082 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL8	Y	0.085 MM	0.085 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL10	Y	0.081 MM	0.081 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
85_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL10	Y	0.057 MM	0.057 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Note: 80ohm copied from 85ohm (pending stack-up calcs)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
80_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL10	Y	0.056 MM	0.056 MM	=STANDARD	0.101 MM	0.101 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.057 MM	?
1x_DIELECTRIC	ISL2,ISL11	0.057 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.057 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.054 MM	?
1x_DIELECTRIC	ISL5,ISL8	0.058 MM	?
1x_DIELECTRIC	ISL6,ISL7	0.051 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

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SYNC MASTER=J43_MLB SYNC DATE=10/24/2012

PAGE TITLE: PCB Rule Definitions

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 32
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_ITP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 16
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 16
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<2..0>	6 16
CPU_CFG3	CPU_45S	CPU_ITP	CPU_CFG<3>	6 16
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..4>	6 16
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 31 64
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 31 32 44
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	15 31 32
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 12 16
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	
(FSB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 44
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 44
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 44
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 44
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 44
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	14 23
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	14 23
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	23 44
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	23 44
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	54
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	54
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	14 44
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	14 44
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 54 44
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 54 44
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_P	26 29
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_N	26 29
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 29
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 29
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	53
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	53
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 53
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 53
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 53
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 53
	DP_80D	DP_AUX	DP_INT_AUX_P	53
	DP_80D	DP_AUX	DP_INT_AUX_N	53

PCIe SSD

DP

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

E85 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
E85_HS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
E85_LS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	*	=6x_DIELECTRIC	?
E85_LS	*	=4x_DIELECTRIC	?
E85_CC	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	TOP,BOTTOM	=10x_DIELECTRIC	?
E85_LS	TOP,BOTTOM	=6x_DIELECTRIC	?
E85_CC	TOP,BOTTOM	=6x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING			
	SPI_45S	SPI	TPAD_SPI_MOSI	15 30	TP SPI
	SPI_45S	SPI	TPAD_SPI_MISO	15 30	
	SPI_45S	SPI	TPAD_SPI_CLK	15 30	
USB_BT	USB_80D	USB	USB_BT_P	14 22	Internal USB
USB_BT	USB_80D	USB	USB_BT_N	14 22	
	USB_80D	USB	USB_BT_R_P	22	
	USB_80D	USB	USB_BT_R_N	22	
USB_BT	USB_80D	USB	USB_BT_CONN_P		
USB_BT	USB_80D	USB	USB_BT_CONN_N		
USB_TPAD	USB_80D	USB	NC_USB_TPADP	14 64	
USB_TPAD	USB_80D	USB	NC_USB_TPADN	14 64	
USB_HPM	USB_85D	USB	USB_HPM_P	28 29	I/O Port Device USB
USB_HPM	USB_85D	USB	USB_HPM_N	28 29	
	USB_85D	USB	USB_HPM_R_P	26	
	USB_85D	USB	USB_HPM_R_N	26	
	USB_80D	USB	USB_EXTA_P	14 26 64	I/O Port Host USB
	USB_80D	USB	USB_EXTA_N	14 26 64	
	USB_85D	USB	USB_EXTA_F_P	26	
	USB_85D	USB	USB_EXTA_F_N	26	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 29 64	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 29 64	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_P		
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_N		
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	29	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	29	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 29	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 29	
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_P	14 27	I/O Port DCI
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_N	14 27	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_P	27 29	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_N	27 29	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_P	14 29	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_N	14 29	
	UART_45S	UART	SMC_DEBUGPRT_TX_L	26 31 32 64	
	UART_45S	UART	SMC_DEBUGPRT_RX_L	26 31 32 64	
USB_EXTB	USB_80D	USB	NC_USB_EXTBP	14 64	USB EXTB nets (Left USB port)
USB_EXTB	USB_80D	USB	NC_USB_EXTBN	14 64	
USB_EXTB	USB_80D	USB	USB2_EXTB_F_P		
USB_EXTB	USB_80D	USB	USB2_EXTB_F_N		
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RP	14 64	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RN	14 64	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P		
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N		
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CP	14 64	
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CN	14 64	
USB_EXTC	USB_80D	USB	USB2_EXTC_P		USB EXTC nets (Left USB port)
USB_EXTC	USB_80D	USB	USB2_EXTC_N		
USB_EXTC	USB_80D	USB	USB2_EXTC_F_P		
USB_EXTC	USB_80D	USB	USB2_EXTC_F_N		
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_P		
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_N		
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_P		
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_N		
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_P		
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_N		
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_P		
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_N		
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_P		
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_N		
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P		
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N		
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N		
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK		

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 31
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 31
	LPC_45S	LPC	LPCPLUS_RESET_L	
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 31
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	
	CLK_LPC_45S	CLK_LPC	TP_LPC_CLK24M_LPCPLUS_R	12 62
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 34
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 34
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 34
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 34
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 31 34 36 53 72
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 31 34 36 53 72
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 40
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 40
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 40
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 40 64
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 40
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 32
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 37
	SPI_45S	SPI	SPI_CLK	37
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 37
	SPI_45S	SPI	SPI_MOSI	37
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 37
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 37
	SPI_45S	SPI	SPI_CS0_L	37
	SPI_45S	SPI	SPI_SMC_CLK	31 37
	SPI_45S	SPI	SPI_SMC_MOSI	31 37
	SPI_45S	SPI	SPI_SMC_MISO	31 37
	SPI_45S	SPI	SPI_SMC_CS_L	31 37
	SPI_45S	SPI	SPI_MLB_CLK	37
	SPI_45S	SPI	SPI_MLB_MOSI	37
	SPI_45S	SPI	SPI_MLB_MISO	37
	SPI_45S	SPI	SPI_MLB_CS_L	37
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	22
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	22
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 22
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 22
	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_P	22
1190	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_N	22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 22
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_P	22
1190	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_N	22
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 62
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 62
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 29 62 64
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 29 62 64
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	24 25
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	24 25
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 25
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 25 64
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 25 64
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	24 25
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	24 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	24 25
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	24 25
1188 PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_P	
1188 PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_N	
1189 DP_TBT_ML	DP_80D	DP_TX	DP_ML_P<3..0>	
1189 DP_TBT_ML	DP_80D	DP_TX	DP_ML_N<3..0>	
1189 DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_P<3..0>	
1189 DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_N<3..0>	
1189 DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_P<3..0>	
1189 DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_N<3..0>	
1189 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_P	
1189 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_N	
1189 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_P	
1189 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_N	
1189 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_P	
1189 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_N	

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK24M_CAMERA	17 24 64
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	24
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

E85 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<0>	5 29
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<0>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<1>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<1>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<3..2>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<3..2>	5 29
	DP_85D	DP_TX	DP_E85SNK_ML_P<3..0>	27 29
	DP_85D	DP_TX	DP_E85SNK_ML_N<3..0>	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_N	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_N	27 29
E85_LS	E85_LS_85D	E85_LS	E85_LS_P<2..1>	26 29 64
E85_LS	E85_LS_85D	E85_LS	E85_LS_N<2..1>	26 29 64
	E85_LS_85D	E85_LS	E85_LS_MISSION_P	26
	E85_LS_85D	E85_LS	E85_LS_MISSION_N	26
		E85_CC	E85_CC1	29 60 64
		E85_CC	E85_CC2	29 60 64

Note: 80ohm constraints are actually 85ohm

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PCH Constraints 2

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_70D
MEM_40S	MEM_TERM	MEM_50S

Note: changed MEM_TERM physical rule to MEM_70D from MEM_73D temporarily

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	? 20
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	? 20
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	? 20
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	? 20
MEM_A_CS0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>	? 20
MEM_A_CS1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>	? 20
MEM_A_ODT	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	? 20 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	? 20
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	? 20
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	? 20 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	? 20 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	? 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	? 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	? 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	? 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	? 20 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	? 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	? 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	? 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	? 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	? 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	? 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	? 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	? 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	? 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	? 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	? 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	? 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	? 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	? 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	? 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	? 20 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	? 20 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	? 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	? 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	? 21 64
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	? 21 64
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	? 21
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	? 21
MEM_B_CS0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>	? 21 64
MEM_B_CS1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>	? 21 64
MEM_B_ODT	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	? 21 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	? 21 64
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	? 21
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	? 21 61 64
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	? 21 61 64
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	? 61 64
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	? 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	? 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	? 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	? 21 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	? 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	? 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	? 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	? 61 64
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	? 61 64
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	? 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	? 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	? 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	? 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	? 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	? 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	? 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	? 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	? 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	? 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	? 21 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	? 21 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	? 61
MEM_B_DQS7	MEM_70D		MEM_B_DQS_N<7>	? 61
		MEM_PWR	PP1V2_S3	8 10 19 20 21 46 52 59 60
		MEM_PWR	PPVREF_S3_MEM_VREFCA	18 19 20 21 69
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A	18 19 20
		MEM_PWR	PPVREF_S3_MEM_VREFCA	18 19 20 21 69
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_B	18 19 21

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Memory Constraints

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NAND BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
NAND_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
NAND_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NAND_DQS	*	0.100 MM	?
NAND_IO	*	0.100 MM	?
NAND_CMD	*	0.100 MM	?

NAND:

DQS_P/N MAX LENGTH 3"
IO<7..0> SIGNALS SHOULD MATCH +/- 50MIL FROM DQS_P/N
IO<7..0> AND ASSOCIATED DQS_P/N ROUTE ON SAME LAYER. NO MORE THAN 2 VIA TRANSITIONS.
NCE<7..0>,ALE,CLE SHOULD MATCH +/- 250MIL FROM NWE
DQS_P/N & NRE_P/N SHOULD MATCH +/- 100MIL FROM NWE

NAND NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
124	ANI0_IO	NAND_45S	NAND_IO	ANI0_IO<7..0>	55 58
124	DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0_DQS_P	55 58
124	DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0_DQS_N	55 58
124	DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0_NRE_P	55 58
125	DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0_NRE_N	55 58
124	ANI0_NWE	NAND_45S	NAND_CMD	ANI0_NWE	55 58
124	ANI0_NCE	NAND_45S	NAND_CMD	ANI0_NCE<3..0>	55 58
124	ANI0_ALE	NAND_45S	NAND_CMD	ANI0_ALE	55 58
124	ANI0_CLE	NAND_45S	NAND_CMD	ANI0_CLE	55 58
125	ANI1_IO	NAND_45S	NAND_IO	ANI1_IO<7..0>	55 58
125	DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1_DQS_P	55 58
125	DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1_DQS_N	55 58
126	DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1_NRE_P	55 58
125	DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1_NRE_N	55 58
126	ANI1_NWE	NAND_45S	NAND_CMD	ANI1_NWE	55 58
126	ANI1_NCE	NAND_45S	NAND_CMD	ANI1_NCE<3..0>	55 58
126	ANI1_ALE	NAND_45S	NAND_CMD	ANI1_ALE	55 58
126	ANI1_CLE	NAND_45S	NAND_CMD	ANI1_CLE	55 58
128	ANI2_IO	NAND_45S	NAND_IO	ANI2_IO<7..0>	
128	DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2_DQS_P	
127	DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2_DQS_N	
128	DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2_NRE_P	
128	DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2_NRE_N	
127	ANI2_NWE	NAND_45S	NAND_CMD	ANI2_NWE	
128	ANI2_NCE	NAND_45S	NAND_CMD	ANI2_NCE<3..0>	
127	ANI2_ALE	NAND_45S	NAND_CMD	ANI2_ALE	
126	ANI2_CLE	NAND_45S	NAND_CMD	ANI2_CLE	
129	ANI3_IO	NAND_45S	NAND_IO	ANI3_IO<7..0>	
129	DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3_DQS_P	
129	DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3_DQS_N	
129	DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3_NRE_P	
129	DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3_NRE_N	
128	ANI3_NWE	NAND_45S	NAND_CMD	ANI3_NWE	
128	ANI3_NCE	NAND_45S	NAND_CMD	ANI3_NCE<3..0>	
128	ANI3_ALE	NAND_45S	NAND_CMD	ANI3_ALE	
128	ANI3_CLE	NAND_45S	NAND_CMD	ANI3_CLE	

NAND NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
130	ANI4_IO	NAND_45S	NAND_IO	ANI4_IO<7..0>	
130	DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4_DQS_P	
129	DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4_DQS_N	
130	DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4_NRE_P	
129	DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4_NRE_N	
130	ANI4_NWE	NAND_45S	NAND_CMD	ANI4_NWE	
129	ANI4_NCE	NAND_45S	NAND_CMD	ANI4_NCE<3..0>	
130	ANI4_ALE	NAND_45S	NAND_CMD	ANI4_ALE	
130	ANI4_CLE	NAND_45S	NAND_CMD	ANI4_CLE	
130	ANI5_IO	NAND_45S	NAND_IO	ANI5_IO<7..0>	
130	DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5_DQS_P	
131	DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5_DQS_N	
131	DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5_NRE_P	
131	DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5_NRE_N	
131	ANI5_NWE	NAND_45S	NAND_CMD	ANI5_NWE	
131	ANI5_NCE	NAND_45S	NAND_CMD	ANI5_NCE<3..0>	
131	ANI5_ALE	NAND_45S	NAND_CMD	ANI5_ALE	
131	ANI5_CLE	NAND_45S	NAND_CMD	ANI5_CLE	
132	ANI6_IO	NAND_45S	NAND_IO	ANI6_IO<7..0>	55 58
132	DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6_DQS_P	55 58
132	DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6_DQS_N	55 58
132	DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6_NRE_P	55 58
132	DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6_NRE_N	55 58
132	ANI6_NWE	NAND_45S	NAND_CMD	ANI6_NWE	55 58
132	ANI6_NCE	NAND_45S	NAND_CMD	ANI6_NCE<3..0>	55 58
133	ANI6_ALE	NAND_45S	NAND_CMD	ANI6_ALE	55 58
133	ANI6_CLE	NAND_45S	NAND_CMD	ANI6_CLE	55 58
133	ANI7_IO	NAND_45S	NAND_IO	ANI7_IO<7..0>	55 58
133	DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7_DQS_P	55 58
133	DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7_DQS_N	55 58
133	DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7_NRE_P	55 58
133	DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7_NRE_N	55 58
133	ANI7_NWE	NAND_45S	NAND_CMD	ANI7_NWE	55 58
134	ANI7_NCE	NAND_45S	NAND_CMD	ANI7_NCE<3..0>	55 58
134	ANI7_ALE	NAND_45S	NAND_CMD	ANI7_ALE	55 58
134	ANI7_CLE	NAND_45S	NAND_CMD	ANI7_CLE	55 58

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NAND CONSTRAINTS

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	24 25
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	24 25
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	24 25
B10	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	24 25 64
B10		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	25
B10	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	24 25
B10	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	24 25
B10	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	24 25
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	24 25
B10	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	24 25
B10	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	24 25
B10	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	24 25
B10	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	24 25
B10	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	24 25 64
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	24 25
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	24 25
B12	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	24 25
B12	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	24 25
B12		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	25 53
B12		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	25 53
B13	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	24 25
B13	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	24 25
B13		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	25 53
B13		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	25 53
B14			S2_MEM_PWR	PP1V35_CAM	24 25
B14			S2_MEM_PWR	PP0V675_CAM_VREF	24 25
B14			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	25

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	0.1 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	31 34 53
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	31 34 53
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 31 34 36 53 68
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 31 34 36 53 68
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL	31 34 46 48
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA	31 34 46 48
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL_R	
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA_R	
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	30 31 34 40
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	30 31 34 40
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	31 34 41 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	31 34 41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_P	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_N	43
	1TO1_DIFFPAIR		CHGR_CSI_R_P	43
	1TO1_DIFFPAIR		CHGR_CSI_R_N	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_P	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_N	43
	1TO1_DIFFPAIR		CHGR_CSO_R_P	43
	1TO1_DIFFPAIR		CHGR_CSO_R_N	43

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P3MM	*	=1TO1_DIFFPAIR	0.300 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.400 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

RF Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
RF_50S	*	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
RF	*	0.15 MM	?

J92 MLB Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
			ISNS_HS_GAIN_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_P
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_N
		SB_POWER	PP3V3_S5
		SB_POWER	PP3V3_S0
		GND	GND
	RF_50S	RF	RF_A_0_DIPLEXER
	RF_50S	RF	RF_A_0_MATCH
	RF_50S	RF	RF_G_0_DIPLEXER
	RF_50S	RF	RF_G_0_MATCH
	RF_50S	RF	RF_0_ANT
	RF_50S	RF	RF_0_ANT_MATCH_T
	RF_50S	RF	RF_A_1_DIPLEXER
	RF_50S	RF	RF_A_1_MATCH
	RF_50S	RF	RF_G_1_DIPLEXER
	RF_50S	RF	RF_G_1_MATCH
	RF_50S	RF	RF_1_ANT
	RF_50S	RF	RF_1_ANT_MATCH_T
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_P<1..0>
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_N<1..0>
	DP_80D	DP_TX	DP_EXT_ML_C_P<1..0>
	DP_80D	DP_TX	DP_EXT_ML_C_N<1..0>
USB_EXTA	USB_80D	USB	DPRUSB_EXTA_P
USB_EXTA	USB_80D	USB	DPRUSB_EXTA_N
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	DPRUSB3_EXTA_D2R_P
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	DPRUSB3_EXTA_D2R_N
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	DPRUSB3_EXTA_R2D_P
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	DPRUSB3_EXTA_R2D_N

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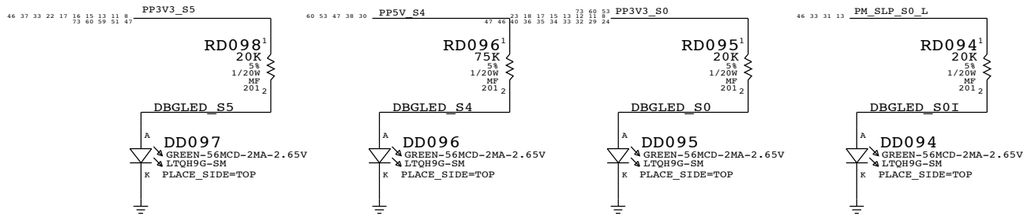
Power State Debug LEDs



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